SG2002

Preliminary Datasheet

Version: 1.0-alpha
Releasedate: 2023-12-15

Revision history

Revision	Date	Description
1.0	2023/12/15	Preliminaryrelease 1.0-alpha

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1 product description

1.1 Overview

SG2002 is a high-performance, low-power chip launched for edge intelligent surveillance IP cameras, smart cat-eye door locks, video doorbells, home intelligence and other product fields. It integrates H.264 video compression codec, H.265 Video compression encoder and ISP; supports HDR wide dynamic range, 3D noise reduction, defogging, lens distortion correction and other image enhancement and correction algorithms to provide customers with professional-level video image quality.

The chip also integrates a self-developed TPU, which can provide 1.0TOPS of computing power under 8-bit integer operations. The specially designed TPU scheduling engine can efficiently provide extremely high bandwidth data flow to all tensor processor cores. In addition, it also provides users with a powerful deep learning model compiler and software SDK development package. Mainstream deep learning frameworks, such as Caffe and Tensorflow, can be easily ported to its platform.

In addition, it also provides secure startup, secure updates, secure encryption, etc., to help users from development, mass production, Product applications, providing a range of security solutions.

An 8-bit MCU subsystem is integrated into the chip, which can replace the general external MCU to save BOM cost and power consumption.

1.2 Architecture

1.2.1 Overview

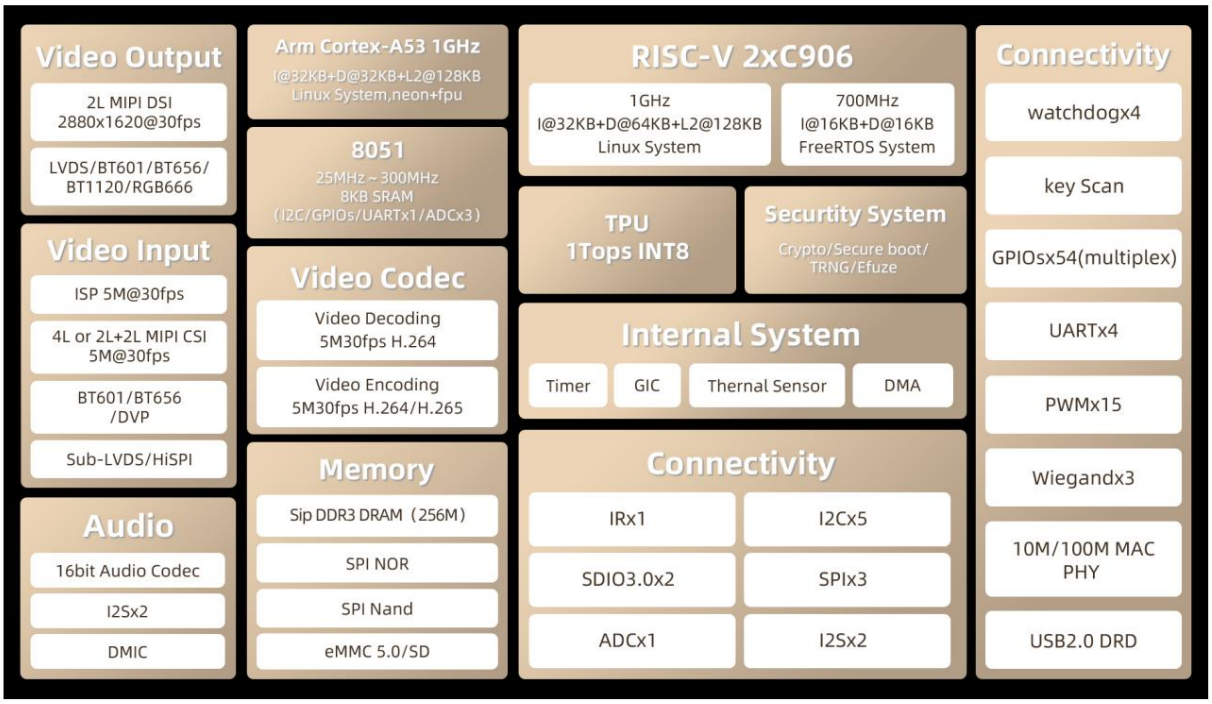


chart ***1-1 SG2002*** block diagram

1.2.2 Processor core

l Main processor RISCVC906@1.0Ghz.

o 32KBI-cache, 64KBD-Cache o Integrated

vector (Vector) and floating point operation unit (FPU). l Main processor ARMCortex-A53@1.0GHz

o 32KBI-cache,32KBD-cache

o 128KBL2 cache

o Support Neon and floating point operation FPU

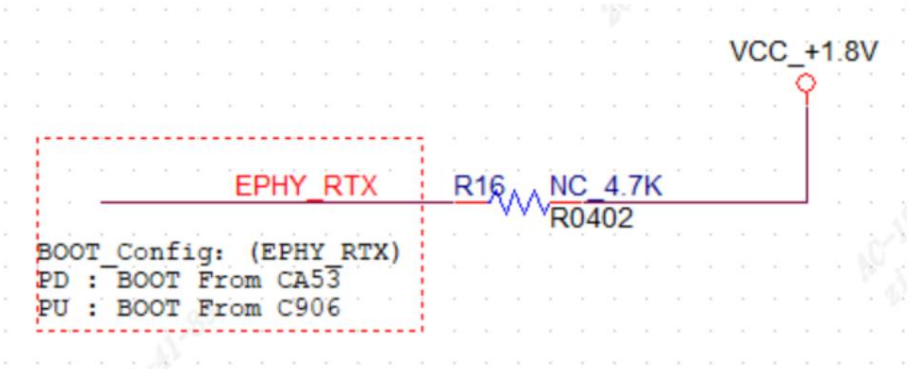
l Co-processor RISCVC906@ 700Mhz o Integrated

floating point unit (FPU).

The main processor RISCVC906@1.0Ghz and the main processor ARMCortex-A53@1.0GHz can be switched through the pin GPIO_RTX__EPHY_RTX. The switching logic is:

Low-------ARMCortex-A53@1.0GHz High------

RISCVC906 @1.0Ghz



1.2.3 TPU

l Built-in TPUl , The computing power reaches ~1.0TOPS INT8
supports mainstream neural network architectures: Caffe, Pytorch, TensorFlow (Lite), ONNX and MXNet l Can realize pedestrian detection (PedestrianDetection), face detection (FaceDetection), face recognition and living (Facerecognition), body detection (Faceanti - spoofing) and other video structuring applications.

1.2.4 Video codec

l H.264Baseline/Main/Highprofile l H.265Mainprofile
l H.264/H.265 supports both I
frame and P frame l MJPEG/JPEGbaseline l
H.264 codec maximum resolution:
2880x1620 (5M) l H.265 encoding Maximum resolution:
2880x1620 (5M) l H.264 encoding and decoding performance
n
2880x1620@30fps+720x576@30fps n 1920x1080@30fps
encoding + 1920x1080@30fps decoding l H.265 encoding performance n

2880x1620@30fps+720x576@30f ps l JPEG Max Codec
performance n 2880x1620@30fps

l Supports multiple rate control modes such as CBR/VBR/FIXQP.
l Supports Region of Interest (ROI) coding

1.2.5 Video interface (SG2002)

l Input n
supports two video inputs at the same time (mipi2L+1L)

n Support MIPI, Sub-LVDS, HiSPI and other serial interfaces.
n Support 8/10/12bitRGBBayer video input. n Support
BT.656 n Support AHD
multi-channel mixed BT format. n Support
SONY, OnSemi, OmniVision and other high-definition CMOS sensors n Supply
The programmable frequency output is used by the sensor as a
reference clock. n supports a maximum width of 2880 and a maximum resolution of 5M (2688x1944, 2880x1620)

l Outputn
supports a variety of serial and parallel screen display
specifications. n Supports serial interfaces
such as MIPI. n Supports parallel interfaces such as BT656, BT601 (8bit), BT1120,
8080, etc. n Supports SPI output interface.

1.2.6 ISP and image processing

l Image and video 90 degree, 180 degree, 270 degree
rotation l Image and video Mirror, Flip function
l Video 2-layer OSD overlay l
Video 1/32~32x zoom function l 3A (AE/
AWB/AF) algorithm l Fixed pattern
noise elimination, Dead pixel correction l Lens
shadow correction, lens distortion correction, purple fringe
correction l Direction adaptive
demosaic l Gamma correction, (regional/global) dynamic contrast enhancement, color
management and enhancement
l Area adaptive defogging l Bayer noise reduction, 3D reduction Noise,
detail enhancement and
sharpening enhancement l LocalTonemapping l
Sensor self-bandwidth dynamic
and 2 frame width dynamic
l Two-axis digital image anti-shake l Lens distortion correction l ISPtuningtools for PC

1.2.7 CV hardware acceleration engine

l The mixed mode of software and hardware supports some OpenCV libraries. l
The mixed mode of software and hardware supports some IVE libraries.

1.2.8 Audio codec (SG2002)

l Integrated AudioCODEC, supports 16bit audio source/voice input and output. l Integrated mono microphone input. l Integrated mono output. (An external power amplifier is required to drive the speaker) l Internally integrated another microphone is directly connected to the output channel, which is convenient Implement AEC. l Software audio codec protocol (G.711, G.726, ADPCM) l Software supports audio 3A (AEC, ANR, AGC) functions.

1.2.9 Network interface

l The Ethernet module provides 1 EthernetMAC. EthernetMAC , Realize the reception and sending of network data. with built-in 10/100Mbps FastEthernetTransceiver can work in 10/100Mbps full-duplex or half-duplex mode.

1.2.10 Security system module

l Hardware implements AES/DES/SM4 multiple encryption and decryption algorithms l Hardware implements HASH (SHA1/SHA256) hash algorithm l Hardware implements random number generator l Internally integrated 2KbiteFuse logical space

1.2.11 Intelligent and safe operating environment

l Support the establishment of trust chain: provide the basis for a secure environment and the basis for a trusted environment, such as hardware security equipment Configuration and root of trust l Support secure boot for secure hardware and software protection functions l Support data encryption security: data encryption program, computing core encryption l Support software and firmware verification process: confirm software credibility and integrity, including booting and Load the signature verification program l Support secure storage and transmission: protect external data storage and exchange l Support secure updates

1.2.12 Peripheral interface (SG2002)

l Integrated POR, Powersequence l 4 single-
ended ADC (3 nodiedomain) l 6 I2C (1nodiedomain)
l 3 SPI l 5 sets of UART (1nodiedomain) l 4
sets (15 channels)
PWM l 2 SDIO interfaces. One supports 3V
Connect to SD3.0Card (support
maximum capacity SDXC2TB,
support speed is UHS-I) One supports 1.8V/3.0V to connect to other SDIO3.0 devices. (Support speed is UHS-I) l 66GPIO interface (14 nodiedomain) l Integrated keyscan and Wiegand l Integrated MACPHY
supports 10/100Mbps full-duplex or half-duplex mode.
l One USBHost/device interface

1.2.13 External memory interface

l Built-in DRAM n
SG2002 DDR316bitx1, maximum speed up to 1866Mbps, capacity 2Gbit (256MB)
l SPINORflash interface (1.8V/3.0V) n Supports 1, 2,
4-wire mode. n Supports a maximum
of 256MByte. l SPINandflash interface
(1.8V/3.0V) n Supports 1KB/2KB/4KBpage
(corresponding maximum capacity 16GB/32GB /64GB) n Use the ECC module built into the
device itself. l eMMC4.5 interface (1.8V/3.0V)
SD0EMMC shares a common power supply. Because the SD card defaults to 3V, there is SD
card, it is not suitable for connecting to
1.8VeMMC. n 4bit
interface. n Supports
HS200 n Maximum supported capacity 2TB

1.2.14 SDK

l Linux-5.10-basedSDK

1.2.15 Chip physical specifications

l Power

consumption n 1080P+Videoencode+AI: ~500mW n Other

scenarios: TBD l Operating

voltage n Core voltage

is 0.9V n IO voltage is 1.8V and

3.0V n DDR voltage is as shown in the

table below. u SG2002 =1.35V l

Package n Use QFN package,

the package

size is 9mmx9mmx0.9mm. The pin pitch is 0.35mm. The total number of pins is 88

1.3 Startup and upgrade mode

1.3.1 Overview

The chip is started by the built-in ROM (BOOTROM). When the chip is reset, it will detect whether there is a weak pull-up or weak pull-down on the two pins (EMMC_DAT3, EMMC_DAT0) to confirm the type of memory device currently selected. Secure boot

chips will be verified during boot and chip upgrade to ensure that the software being executed or upgraded is safe.

1.3.2 Correspondence between startup mode and corresponding signal latch value

l Support startup by SPINorFlash (EMMC_DAT3pulldown, EMMC_DAT0pullup) l Support startup by SPINandFlash (EMMC_DAT3pulldown, EMMC_DAT0pulldown) l Support startup by eMMC (EMMC_DAT3pullup, EMMC_DAT0pullup)

Note.SG2002 Because SD0 and eMMCdomain share IOpower. Because the SD card defaults to 3.0V, and Most eMMC is 1.8V, so it basically does not support eMMC unless SD0 does not connect to the SD card.

1.3.3 Image burning mode.

l Supports image burning through SD card. l

Supports image burning through USBdevicemode. l If there is an

image in flash, the software supports software upgrade through the network

1.3.4 Secure boot

l Support secure boot and upgrade
l AES/DES/SM4 hardware encryption and
decryption. l SHA/TRNG/SecureEfuse security hardware.

1.4 Address space mapping

Start address [31:0]	End address [31:0]	Space function	Space size (Byte)
0x01000000	0x017FFFFF	reserved	8M
0x01800000	0x018FFFFF	reserved	
0x01900000	0x01900FFF	ap_mailbox	4K
0x01901000	0x01901FFF	ap_system_ctrl	4K
0x01902000	0x019EFFFF	reserved	
0x01F00000	0x01F0FFFF	reserved	64K
0x01F10000	0x01FFFFFF	reserved	
0x02000000	0x02FFFFFF	reserved	64K
0x03000000	0x03000FFF	TOP_MISC control register	4K
0x03001000	0x03001FFF	PINMUX control register	4K
0x03002000	0x03002FFF	CLKGEN/PLL control register	4K
0x03003000	0x03003FFF	RSTGEN control register	4K
0x03004000	0x03005FFF	reserved	
0x03006000	0x03006FFF	reserved	4K
0x03007000	0x03008FFF	reserved	
0x03009000	0x03009FFF	reserved	4K
0x0300A000	0x0300AFFF	reserved	4K
0x0300B000	0x0300FFFF	reserved	
0x03010000	0x03010FFF	WATCHDOG0 control register	4K
0x03011000	0x03011FFF	WATCHDOG1 control register	4K
0x03012000	0x03012FFF	WATCHDOG2 control register	4K
0x03020000	0x03020FFF	GPIO0 control register	4K
0x03021000	0x03021FFF	GPIO1 control register	4K
0x03022000	0x03022FFF	GPIO2 control register	4K
0x03023000	0x03023FFF	GPIO3 control register	4K
0x03024000	0x0302FFFF	reserved	
0x03030000	0x03030FFF	WGN0 control register	4K
0x03031000	0x03031FFF	WGN1 control register	4K
0x03032000	0x03032FFF	WGN2 control register	4K
0x03033000	0x0303FFFF	reserved	
0x03040000	0x0304FFFF	KEYSCAN control register	64K
0x03050000	0x0305FFFF	EFUSE control register	64K
0x03060000	0x03060FFF	PWM0 control register	4K
0x03061000	0x03061FFF	PWM1 control register	4K
0x03062000	0x03062FFF	PWM2 control register	4K
0x03063000	0x03063FFF	PWM3 control register	4K
0x03064000	0x0309FFFF	reserved	

0x030A0000	0x030AFFFF	TIMER control register	64K
0x030C0000	0x030CFFFF reserved		
0x030D0000	0x030D0FFF reserved		4K
0x030D1000	0x030D1FFF reserved		4K
0x030D2000	0x030D2FFF reserved		4K
0x030D3000	0x030DFFFF reserved		
0x030E0000	0x030EFFFF	TEMPSEN control register	64K
0x030F0000	0x030FFFFF	SARADC control register	64K
0x04000000	0x0400FFFF	I2C0 control register	64K
0x04010000	0x0401FFFF	I2C1 control register	64K
0x04020000	0x0402FFFF	I2C2 control register	64K
0x04030000	0x0403FFFF	I2C3 control register	64K
0x04040000	0x0404FFFF	I2C4 control register	64K
0x04050000	0x0405FFFF reserved		
0x04060000	0x0406FFFF	SPI_NAND control register	64K
0x04070000	0x0407FFFF	ETH0 control register	
0x04080000	0x040FFFFF reserved		
0x04100000	0x04107FFF	I2S0 control register	64K
0x04108000	0x0410FFFF	I2SGlobal control register	64K
0x04110000	0x0411FFFF	I2S1 control register	64K
0x04120000	0x0412FFFF	I2S2 control register	64K
0x04130000	0x0413FFFF	I2S3 control register	64K
0x04140000	0x0414FFFF	UART0 control register	64K
0x04150000	0x0415FFFF	UART1 control register	64K
0x04160000	0x0416FFFF	UART2 control register	64K
0x04170000	0x0417FFFF	UART3 control register	64K
0x04180000	0x0418FFFF	SPI0 control register	64K
0x04190000	0x0419FFFF	SPI1 control register	64K
0x041A0000	0x041AFFFF	SPI2 control register	64K
0x041B0000	0x041BFFFF	SPI3 control register	64K
0x041C0000	0x041CFFFF	UART4 control register	64K
0x041D0000	0x041DFFFF AUDSRC control register		64K
0x041E0000	0x042FFFFF reserved		
0x04300000	0x0430FFFF eMMC control register		64K
0x04310000	0x0431FFFF	SD0 control register	64K
0x04320000	0x0432FFFF SD1 control register		
0x04330000	0x0433FFFF DMA control register		64K
0x04340000	0x0434FFFF	USB control register	64K
0x04350000	0x043FFFFF reserved		
0x04400000	0x0441FFFF ROM memory space		128K
0x04420000	0x04FFFFFF reserved		

0x05000000	0x05000FFF reserved		4KB
0x05020000	0x05020FFF	RTCSYS_Timer control register	4KB
0x05021000	0x05021FFF	RTCSYS_GPIO control register	4KB
0x05022000	0x05022FFF	RTCSYS_UART control register	4KB
0x05023000	0x05023FFF	RTCSYS_INTR control register	4KB
0x05024000	0x05024FFF	RTCSYS_MBOX control register	4KB
0x05025000	0x05025FFF	RTCSYS_CTRL control register	4KB
0x05026000	0x05026FFF	RTCSYS_CORE	4KB
0x05027000	0x05027FFF	RTCSYS_IO control register	4KB
0x05028000	0x05028FFF	RTCSYS_OSC control register	4KB
0x05029000	0x05029FFF reserved		4KB
0x0502A000	0x0502AFFF	RTCSYS_32kless control register	4KB
0x0502B000	0x0502BFFF	RTCSYS_I2C control register	4KB
0x0502C000	0x0502CFFF	RTCSYS_SAR control register	4KB
0x0502D000	0x0502DFFF RTCSYS_WDT control register		4KB
0x0502E000	0x0502EFFF	RTCSYS_IRRX control register	4KB
0x05200000	0x053FFFFF	RTCSYS_SRAM	8KB
0x05400000	0x057FFFFF	RTCSYS_SPINOR	4MB
0x08000000	0x08001FFF reserved		8K
0x08004000	0x08005FFF DDRControler control register		8K
0x08006000	0x08007FFF reserved		8K
0x08008000	0x08009FFF DDRAXIMonitor control register		8K
0x0800A000	0x0800BFFF DDRGlobal control register		8K
0x08010000	0x08011FFF reserved		8K
0x08012000	0x08013FFF reserved		8K
0x08014000	0x09FFFFFF reserved		
0x0A000000	0x0A07FFFF	ISP control register	512K
0x0A080000	0x0A0803FF	sc_top control register	1K
0x0A080400	0x0A080BFF reserved		2K
0x0A080C00	0x0A080CFF	osdenc control register	256B
0x0A080D00	0x0A080FFF Reserved		768B
0x0A081000	0x0A081FFF reserved		4K
0x0A082000	0x0A082FFF	img_v control register	4K
0x0A083000	0x0A083FFF	img_d control register	4K
0x0A084000	0x0A084FFF	sc_d control register	4K
0x0A085000	0x0A085FFF	sc_v1 control register	4K
0x0A086000	0x0A086FFF	sc_v2 control register	4K
0x0A087000	0x0A087FFF	sc_v3 control register	4K
0x0A088000	0x0A088FFF	DISP control register	4K
0x0A089000	0x0A089FFF Reserved		4K
0x0A08A000	0x0A08AFFF	dsi_mac control register	4K

0x0A08B000	0x0A08BFFF	cmdq control register	4K
0x0A08C000	0x0A08CFFF	reserved	4K
0x0A08D000	0x0A08DFFF	reserved	4K
0x0A08E000	0x0A09FFFF	reserved	72K
0x0A0A0000	0x0A0AFFFF	IVE control register	64K
0x0A0A0000	0x0A0BFFFF	reserved	64K
0x0A0C0000	0x0A0C1FFF	ldc control register	8K
0x0A0C2000	0x0A0C3FFF	VI0/MIPI_RX0 control register	8K
0x0A0C4000	0x0A0C5FFF	VI1/MIPI_RX1 control register	8K
0x0A0C6000	0x0A0C7FFF	VI2/MIPI_RX2 control register	8K
0x0A0C8000	0x0A0C9FFF	VIPSYS control register	8K
0x0A0CA000	0x0A0CFFFF	reserved	24K
0x0A0D0000	0x0A0D0FFF	CSI_PHY control register	4K
0x0A0D1000	0x0A0D1FFF	DSI_PHY control register	4K
0x0A0D2000	0x0AFFFFFF	reserved	
0x0B000000	0x0B00FFFF	JPEGcodec control register	64K
0x0B010000	0x0B01FFFF	H.264codec control register	64K
0x0B020000	0x0B02FFFF	H.265codec control register	64K
0x0B030000	0x0BFFFFFF	reserved	
0x0C000000	0x0FFFFFFF	reserved	
0x10000000	0x1FFFFFFF	SPI_NOR memory space	256M
0x30000000	0x7FFFFFFF	reserved	
0x80000000	0xFFFFFFFF	DDR memory space	2G

*Reading and writing operations on the reserved address space may produce unpredictable results.

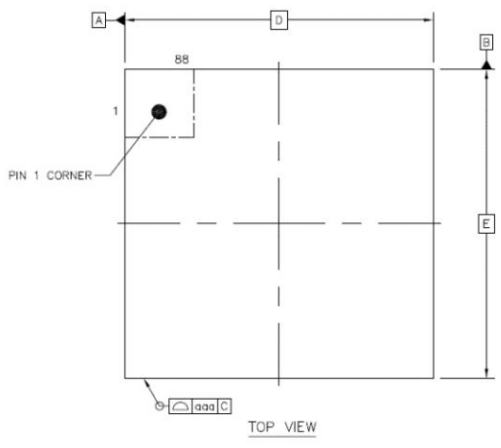
2 Hardware features

2.1 Package and pin distribution

2.1.1 Package **SG2002**

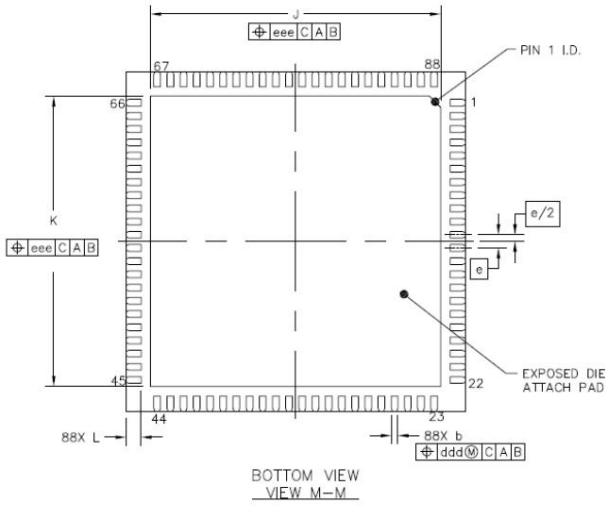
SG2002 uses QFN package, the package size is 9mmx9mmx0.9mm. The pin pitch is 0.35mm.

The total number is 88. Please refer to the figure below for detailed package dimensions.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

chart ***2-1 SG2002*** Package appearance dimensions top view



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

chart ***2-2.SG2002*** Package appearance dimensions bottom view

2.1.2 Pin distribution **SG2002**

		88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	
		PAD_MIPI_TXP0	PAD_MIPI_TXM0	PAD_MIPI_TXP1	PAD_MIPI_TXM1	PAD_MIPI_TXP2	PAD_MIPI_TXM2	VDD18A_MIPI	PAD_MIPIRX0P	PAD_MIPIRX0N	PAD_MIPIRX1P	PAD_MIPIRX1N	PAD_MIPIRX2P	PAD_MIPIRX2N	PAD_MIPIRX3P	PAD_MIPIRX3N	PAD_MIPIRX4P	PAD_MIPIRX4N	VDDC	USB_DM	USB_DP	VDD18A_USB_PLL_ETH	GPIO_RTX___EPHY_RTX	
VSS18A_AUD	1																							66 VDD33A_ETH_USB
PAD_AUD_AINL_MIC	2																							65 PAD_ETH_RXM___EPHY_TXP
PAD_AUD_AVREF	3																							64 PAD_ETH_RXP___EPHY_TXN
PAD_AUD_AOUTR	4																							63 PAD_ETH_TXM___EPHY_RXP
VDD18A_AUD	5																							62 PAD_ETH_TXP___EPHY_RXN
SD0_CLK	6																							61 VDDC
SD0_CMD	7																							60 USB_VBUS_DET
SD0_D0	8																							59 ADC1
VDDC	9																							58 PWM0_BUCK
SD0_D1	10																							57 VDDIO_SD1
SD0_D2	11													VSSC (EPAD)										56 SD1_CLK
SD0_D3	12																							55 SD1_CMD
VDDIO_SD0_EMMC	13																							54 SD1_D0
SD0_CD	14																							53 SD1_D1
SD0_PWR_EN	15																							52 SD1_D2
VDDC	16																							51 SD1_D3
SPK_EN	17																							50 VDDC
UART0_TX	18																							49 PWR_GPIO2
UART0_RX	19																							48 PWR_GPIO1
EMMC_DAT2	20																							47 PWR_GPIO0
EMMC_CLK	21																							46 XTAL_XOUT
EMMC_DAT0	22																							45 XTAL_XIN
		23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	
		EMMC_DAT3	EMMC_CMD	EMMC_DAT1	JTAG_CPU_TMS	JTAG_CPU_TCK	IIC0_SCL	IIC0_SDA	AUX0	VDDQ_DRAM	VDDQ	VDDQ	VDDQ_DRAM	GPIO_ZQ___PAD_ZQ	VDDIO_RTC	VDDC_RTC	PWR_VBAT_DET	PWR_RSTN	PWR_SEQ1	PWR_SEQ2	PTEST	PWR_WAKEUP0	PWR_BUTTON1	

chart ***2-3 SG2002*** Pin layout diagram

2.2 Description of pin information

Please refer to SG2002_PINOUT_CN.xlsx

2.3 Welding process recommendations

Please refer to chart 2-4 for the lead-free reflow soldering process curve.

SG2002 Please refer to PureSn

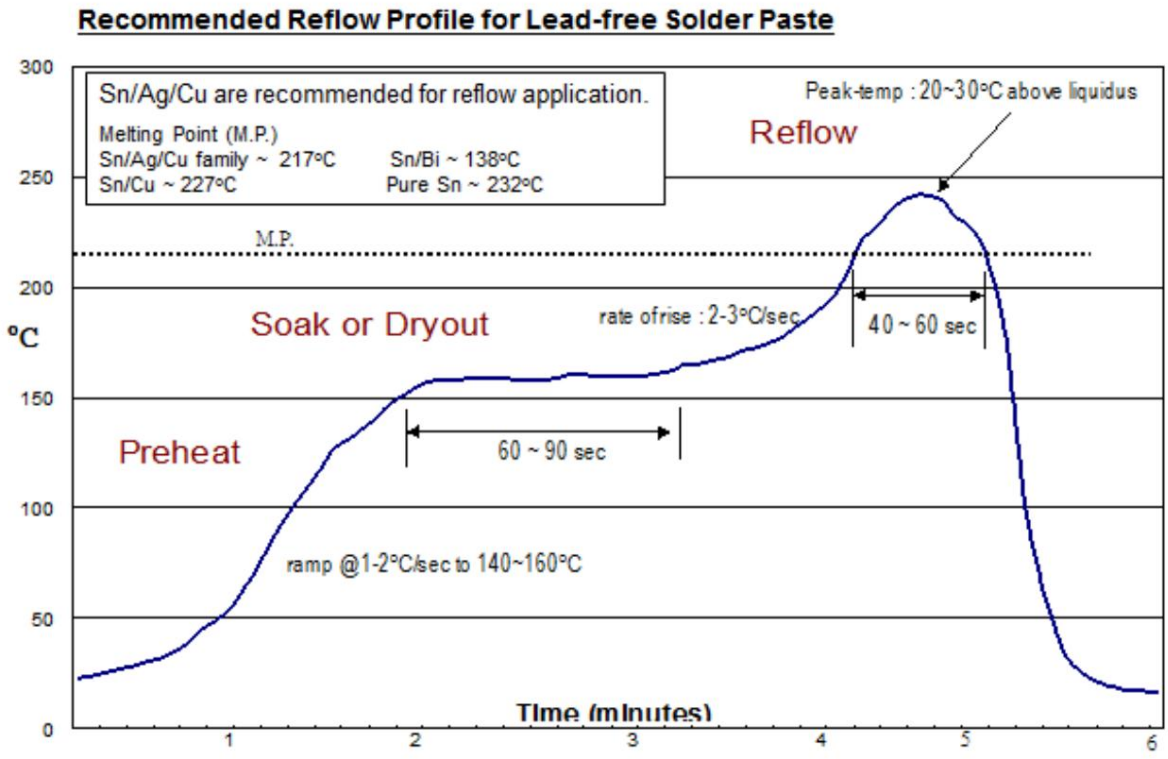


chart **24** Lead-free reflow soldering process curve

Please refer to Table 2ÿ1 for lead-free reflow soldering process parameters.

l The following parameters are only recommended values for reference, and the client needs to make corresponding adjustments based on actual production conditions.

sheet **2 1** Lead-free reflow soldering cap parameters

Regional time heating rate peak temperature preheating zone **(40~150o C)** 60~120sc				cooling rate
1~2o C/sec **Average temperature zone (150~200o C)** 60~90sec				
< 1o C/sec				
Reflow area (>melting point **20~30o C)**	40~60sec 2~3o C/sec		Sn/Ag/Cu237~ 247oC Sn/Cu247~ 257oC PureSn252~262o C	
cooling zone **(Tmax~Also)**				1~4o C/sec

Due to environmental protection reasons, parameters for lead-containing reflow soldering are currently not available.

2.4 Moisture sensitive parameters

2.4.1 Moisture-proof packaging of Shuuneng products

This chapter formulates the principles for the storage and soldering of chips (moisture-sensitive products).

Related terms l Floorlife (opening storage time): refers to the period between unpacking the moisture-proof packaging and reflowing in an environment <30oC/60%RH Maximum length of stay allowed.

l Shelflife (sealed storage time): the normal storage time after the moisture-proof packaging is sealed.

2.4.1.1 Packaging information

The moisture-proof vacuum bag contains (1) chip and tray. (2) drying bag (3) humidity card (HIC)

chart 2-5 Vacuum drying packaging information

chart **2-6** Drying package humidity card chip and **tray** plate

2.4.1.2 Incoming inspection of moisture-sensitive products

After opening the vacuum moisture-proof bag before SMT, check the humidity card. There are many different styles of humidity cards. But if it shows If it is exposed to moisture, it must be baked before SMT can be used. Please see Table 2ÿ3 for the relevant baking time and temperature parameters.

If repackaged after opening and not exposed to an environment <30o C/60%RH for more than 2 hours, you can only replace it. After changing the drying bag, carry out vacuum drying and packaging. If it exceeds 2 hours, it is recommended to re-bake and replace the drying bag before resealing. Seal packaging.

2.4.1.3 Storage and use. (Refer to **JEDEC J-STD-033)**

l Sealed storage time.(Shelflife)

Sealed vacuum moisture-proof bags, stored in an environment of 40o C/90%RH, can be stored for at least 12 months.

l Storage time after opening.(Floorlife)

Before SMT, the hygrometer shows that there are no damp components after opening. In an environment of 30o C/60%RH, drying is not required.

The time for direct use after baking is as shown in Table 2-2 Level 3 (the Floorlife rating of this chip is Level 3)

sheet **2 . 2** Humidity classification and storage time after opening ***(floorlife)***

Moisture classification level and floor life

Level	Floor Life (out of bag) at factory ambient ≤ 30 °C/60% RH or as stated
1	Unlimited at ≤ 30 °C/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

2.4.1.4 Rebaking

If it is found that it has become damp after opening, it should be baked first before SMT, or if it is to be put back into the vacuum package. The baking temperature should be

For temperature and time, please refer to

Table 2-3. After baking and moisture-proof sealing, shelflife can be recalculated.

After baking, if it is not sealed against moisture, please refer to the storage time (floorlife)

sheet 2 . 3 Baking temperature and timetable

Package Thickness	Level	Bake @ 125 °C	Bake @ 40 °C ≤ 5% RH
≤ 1.4 mm	2a	4 h.	5 days
	3	7 h.	11 days
	4	9 h.	13 days
	5	10 h.	14 days
	5a	14 h.	19 days
≤ 2.0 mm	2a	18 h.	21 days
	3	24 h.	33 days
	4	31 h.	43 days
	5	37 h.	52 days
	5a	48 h.	68 days
≤ 4.0 mm	2a	48 h.	67 days
	3	48 h.	67 days
	4	48 h.	68 days
	5	48 h.	68 days
	5a	48 h.	68 days

2.5 Electrical performance parameters

2.5.1 Power consumption parameters

Typical scenario: 1080P+VideoEncode+AI~500mW

Other scenes: TBD

2.5.2 Temperature and thermal resistance parameters (SG2002)

The thermal resistance of the chip ThetaJA, JB, JC values. According to the results of JEDEC2s2pPCB, Table 2-4

sheet 2 ' 4 SG2002 Thermal resistance parameters

PCB Condition	Package Size(mm)	ThetaJA(C/W)			PsiJt (C/W)	ThetaJC (C/W)	ThetaJB (C/W)
		0m/s	1m/s	2m/s			
JEDEC 2s2pPCB	9x9	20.3	15.9	14.8	0.17	6.9	5.32

The temperature-related parameters of the chip are shown in Table 2-5

sheet 2 ' 5 Temperature related parameters

	Minimum	Maximum	Note
Working environment temperature **Tamb** chip			1
junction temperature **Tjunc** recommended value	-30o C	70o C 85o C~105o	2
destructive junction temperature	-30o C -40o C	C +125o C	3,4

1. The maximum working environment temperature, without violating the junction temperature, depends on the power consumption and heat dissipation conditions of the scenario.

2. The recommended range of chip junction temperature mainly considers that when the temperature is too high, thermal may be caused due to poor heat dissipation conditions.
run-away causes the temperature to be out of control and enter the destructive junction temperature range and damage the chip. In addition, working at high temperatures for a long time will also
It will slightly accelerate chip aging and reduce the service life.

3. The guaranteed junction temperature of the DRAM used is only -40o C~115o C. If it exceeds the range, the content in the DRAM cannot be guaranteed to be complete.
sex.

4. When the chip operates at a destructive junction temperature, it may cause irreversible physical damage to the chip.

2.5.3 Destructive voltage

The destructive voltage parameters are shown in Table 2-6. When working above the destructive voltage, irreversible physical damage may be caused.

sheet 2 6 Destructive voltage parameters **(SG2002)**

Parameter		Max	Unit
VDDC	Corepower	1.05V	IN
VDDC_RTC	CorepowerforRTCdomain (comes with LDO)		
VDD18A_AUD	AnalogpowerforAudioADC/DAC	1.98	IN
VDD18A_USB_PLL_ETH	AnalogpowerforUSB,PLL,ETH,efuse	1.98	IN
VDD18A_MIPI	AnalogpowerforMIPI	1.98	IN
VDD33A_ETH_USB	AnalogpowerforEthernetPHY,USBPHY	3.465	IN
VDDIO_SD0_EMMC	IOpowerforEMMC&SD0domain	3.465	IN
VDDIO_SD1	IOpowerforSD1domain	3.465	IN
VDDIO_RTC	IOpowerforRTCdomain(backuppower)	1.98	IN
VDDQ **VDDQ_DRAM**	IO&DRAMPowerforDDR2/DDR3L/DDR3	1.65	IN

2.5.4 Power on and off sequence **(SG2002)**

In principle, chips can be divided into the following groups. The power domain of the same group is powered on/off at the same time. Different groups, according to the following conditions:

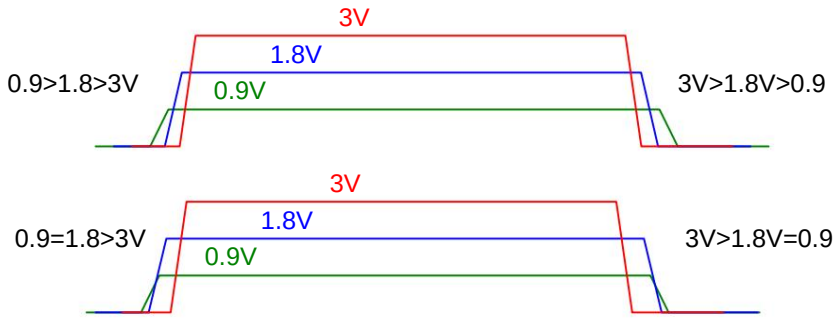
Separate the power-on and power-off times.

l Alwaysondomain
  n VDDIO_RTC(1.8V)
  n VDDC_RTC(0.9V)(built-in LDO)
  n VDDIO_SD1
l Corepowerdomain
  n VDDC
l 1.8VIOdomain
  n VDD18A_AUD(analog)
  n VDD18A_USB_PLL_ETH(analog)
  n VDD18A_MIPI(analog)
l 18OD33IOdomain (it depends on the voltage to determine whether it belongs to 1.8Vdomain/3Vdomain)
  n VDDIO_SD1 (also nodiedomain)
l 3Vdomain
  n VDDIO_SD0_EMMC
  n VDD33A_ETH__USB
l DDRIO&DRAMdomain
  n VDDQ

n VDDQ_DRAM

In principle, 0.9V and 1.8V can be powered on at the same time, or 0.9V first and then 1.8V, but **3V** must be established before **1.8V.**

Power can only be powered on if the prerequisites are established. (Violation of the order may cause irreversible damage) . Powering off is the reverse order of powering on.



Power-on and power-down behaviors that may

cause risks include: 1. When powering up, if VDD3 is >2V, VDD18 has not yet reached 1.8V-10%. This may cause damage to the 3V circuit. 2. When , VDD18 is lower than 1.8V-10%.

powering off, if VDD3 is <2V 3. When powering down, when VDD18>0.7V, but VDD09 is still below 0.5V, it may cause efuse malfunction. 4. When powering down, when VDD09<0.5V, VDD18 is still >0.7V, it may also cause efuse to malfunction.

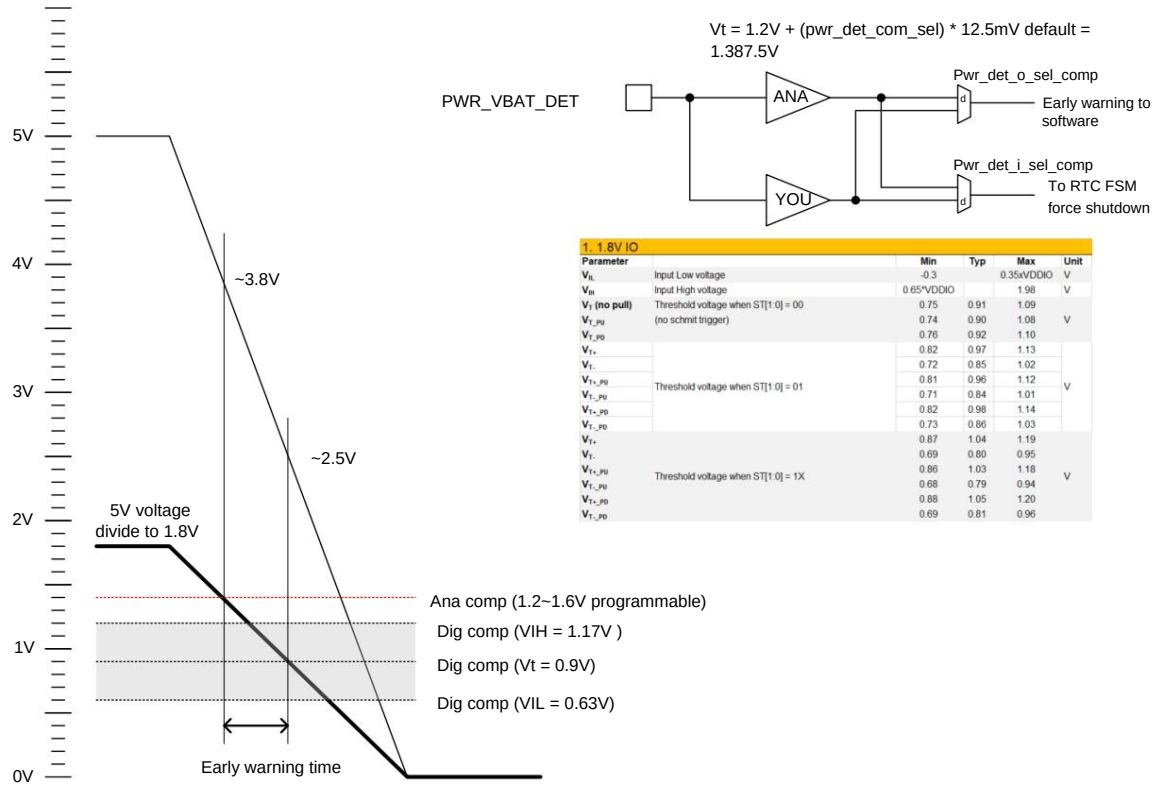
The chip has two pins PWR_SEQ1 and PWR_SEQ2 (VDDIO_RTCdomain) to help control the power switch. The default SEQ1 is 0.9V & 1.8V. SEQ2 controls 3V. Some plug-in systems may use RC to determine the switch between 0.9V and 1.8V. .I only hope that the 3V of the chip still needs to be controlled by SEQ2 to avoid burning it.

SEQ1->SEQ2 when turning on

SEQ2->SEQ1 when turning off

PWR_VBAT_DET is used to detect the status of the main power supply. If the voltage is low, the software will receive an interrupt first (for example For example, stop writing to flash to prevent file system damage). If the voltage drops further, the RTC module will automatically start the power-off process.

PWR_VBAT_DET also needs to be logichigh to boot.



1. 1.8V IO

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.35xVDDIO	V
V_{IH}	Input High voltage	0.65*VDDIO		1.98	V
V_T (no pull)	Threshold voltage when ST[1:0] = 00	0.75	0.91	1.09	
V_{T_PU}	(no schmit trigger)	0.74	0.90	1.08	V
V_{T_PD}		0.76	0.92	1.10	
V_{T+}		0.82	0.97	1.13	
V_{T-}		0.72	0.85	1.02	
V_{T+_PU}	Threshold voltage when ST[1:0] = 01	0.81	0.96	1.12	V
V_{T-_PU}		0.71	0.84	1.01	
V_{T+_PD}		0.82	0.98	1.14	
V_{T-_PD}		0.73	0.86	1.03	
V_{T+}		0.87	1.04	1.19	
V_{T-}		0.69	0.80	0.95	
V_{T+_PU}	Threshold voltage when ST[1:0] = 1X	0.86	1.03	1.18	V
V_{T-_PU}		0.68	0.79	0.94	
V_{T+_PD}		0.88	1.05	1.20	
V_{T-_PD}		0.69	0.81	0.96	

In actual use, the following four situations can be subdivided. The suggestions are as follows.

Power	Control	Plug-in applications(1) **ExtRTC/noRTC**	Plug-in applications(2) **32Kless**
Main0.9V	Alwayson VDDC		VDDC
Main1.8V	Alwayson	VDD18A_AUD VDD18A_USB_PLL_ETH VDD18A_MIPI VDDIO_SD1 VDDIO_RTC	VDD18A_AUD VDD18A_USB_PLL_ETH VDD18A_MIPI
Main3.0V SEQ2		VDD33A_ETH_USB VDDIO_SD0_EMMC VDDIO_SD1	VDD33A_ETH_USB VDDIO_SD0_EMMC
MainVDDQ alwayson		VDDQ VDDQ_DRAM	VDDQ VDDQ_DRAM
VDDBACKUP CoinBatt		ForexternalRTC	
V18RTC(lowiddqLDO)	AlwaysonfromCoinbatt	Noneed	VDDIO_RTC VDDIO_SD1

Power	Control	Battery Application(3) ExtRTC/noRTC	Battery Application(4) 32Kless
Main0.9V SEQ1		VDDC	VDDC
Main1.8V SEQ1		VDD18A_AUD VDD18A_USB_PLL_ETH VDD18A_MIPI	VDD18A_AUD VDD18A_USB_PLL_ETH VDD18A_MIPI
Main3.0V SEQ2		VDD33A_ETH_USB VDDIO_SD0_EMMC	VDD33A_ETH_USB VDDIO_SD0_EMMC
MainVDDQ SEQ2or3		VDDQ VDDQ_DRAM	VDDQ VDDQ_DRAM
VDDBACKUP CoinBatt		ForexternalRTC	
V18RTC(lowiddqLDO)	, AlwaysonfromCoinbatt	Noneed	VDDIO_RTC
VAO18	fromMain batt	WIFI otherAOdevice VDDIO_RTC VDDIO_SD1	WIFI otherAOdevice VDDIO_SD1
VAO33	fromMainbatt	WIFI otherAOdevice	WIFI otherAOdevice

2.5.5 Power supply **DC/AC** electrical parameters

sheet 2 7 SG2002 Power Supply Electrical Parameters Recommended Operating Conditions)

Parameter		Min	Type	Max	Unit
VDDC	Corepower	0.81	0.9	0.99	IN
VDDC_RTC	CorepowerforRTCdomain(InternalLDO,Caponly)	0.81	0.9	0.99	IN
VDD18A_AUD	AnalogpowerforAudioADC/DAC	1.62	1.8	1.98	IN
VDD18A_USB_PLL_ETH	AnalogpowerforEthernetPHY,USBPHY,PLL	1.62	1.8	1.98	IN
VDD18A_MIPI	AnalogpowerforMIPI	1.62	1.8	1.98	IN
VDD33A_ETH_USB	AnalogpowerforEthernetPHY,USBPHY	2.97	3.3	3.465	IN
					IN
VDDIO_SD0_EMMC	IOpowerforSD0&EMMCdomain	1.71 2.85	1.8 3.0/3.3	1.89 3.15/3.465	IN
VDDIO_SD1	IOpowerforSD1domain	1.71 2.85	1.8 3.0/3.3	1.89 3.465	IN

Parameter		Min	Type	Max	Unit
VDDIO_RTC	IOpowerforRTCdomainIO&LDO	1.3V	1.8	+10%	IN
VDDQ **VDDQ_DRAM**	IO&DRAMPowerforDDR3L IO&DRAMPowerforDDR3 IO&DRAMPowerforDDR2	1.283 1.425 1.425	1.35 1.50 1.50	1.417 1.575 1.575	IN
Tjunc	JunctionTemperature(Maxreducefrom125Cdueto DRAM)	-40	25	115 (note)	°C

Note. The guaranteed junction temperature of the DRAM used is only -40o C~115o C. Beyond this range, the content in the DRAM cannot be guaranteed to be complete.

Wholeness.

2.5.6 1.8V IO electrical parameters

Applicable domain(VDDIO18_0,VDDIO18_1,VDDIO18_RM0,VDDIO_RTC)

sheet 2 8 1.8VIO Electrical parameters

Parameter		Min	Type	Max	Unit
WILL	InputLowvoltage	-0.3		0.35xVDDIO	IN
HIV	InputHighvoltage	0.65*VDDIO		1.98	IN
VT (no pull)	ThresholdvoltagewhenST[1:0]=00(noschmittrigger)	0.75	0.91	1.09	
VT_PU		0.74	0.90	1.08	IN
VT_PD		0.76	0.92	1.10	
VT+	ThresholdvoltagewhenST[1:0]=01	0.82	0.97	1.13	
VT-		0.72	0.85	1.02	
VT+_PU		0.81	0.96	1.12	
VT-_PU		0.71	0.84	1.01	IN
VT+_PD		0.82	0.98	1.14	
VT-_PD		0.73	0.86	1.03	
VT+	ThresholdvoltagewhenST[1:0]=1X	0.87	1.04	1.19	
VT-		0.69	0.80	0.95	
VT+_PU		0.86	1.03	1.18	
VT-_PU		0.68	0.79	0.94	IN
VT+_PD		0.88	1.05	1.20	
VT-_PD		0.69	0.81	0.96	
~	Input leakage(VI =1.8Vor0V)			+/-10u	A
IOZ	Tri-stateoutputleakagecurrent(VO=1.8Vor0V)			+/-10u	A
RPU	Pullupresistor	55k	79k	121k	Oh
RPD	Pulldownresistor	51k	87k	169k	Oh
VOL	Outputlowvoltage			0.45	IN
VOH	Outputhighvoltage	1.35			IN
IOL	Lowleveloutputcurrent@VOL (max)				
	DS[1:0]=00	7.6	12.8	18.0	mA
	DS[1:0]=01	15.2	25.3	35.5	mA
	DS[1:0]=10	22.6	37.4	52.2	mA
	DS[1:0]=11	29.7	49	67.9	mA
John	Highleveloutputcurrent@ VOH (max)				
	DS[1:0]=00	4.8	10.8	18.9	mA
	DS[1:0]=01	9.5	21.5	37.4	mA
	DS[1:0]=10	14.3	32.1	55.9	mA
	DS[1:0]=11	18.9	42.4	73.9	mA

2.5.7 18OD33 IO (VDDIO=1.8V) electrical parameters

Applicable domain(VDDIO_EMMC,VDDIO_SD0)

sheet 2 9 18OD33IO(VDDIO=1.8V) Electrical parameters

Parameter		Min	Type	Max	Unit
WILL	Input Lowvoltage	-0.3		0.58	IN

Parameter		Min	Type	Max	Unit
HIV	InputHighvoltage	1.27		2.00	IN
VT (no pull)	ThresholdvoltagewhenST=0(noschmittrigger)	0.91	0.97	1.03	
VT_PU		0.90	0.96	1.02	IN
VT_PD		0.91	0.97	1.06	
VT+ (no pull)	ThresholdvoltagewhenST=1	1.03	1.07	1.12	
VT- (nopull)		0.75	0.83	0.91	
VT+_PU		1.02	1.06	1.11	IN
VT-_PU		0.74	0.82	0.90	
VT+_PD		1.03	1.08	1.13	
VT-_PD		0.75	0.83	0.92	
~	Input leakage(VI =1.8Vor0V)			+/-10u	A
IOZ	Tri-stateoutputleakagecurrent(VO=1.8Vor0V)			+/-10u	A
RPU	Pullupresistor	33k	60k	92k	Oh
RPD	Pulldownresistor	34k	61k	158k	Oh
VOL	Outputlowvoltage			0.45	IN
VOH	Outputhighvoltage	1.40			IN
IOL	Lowleveloutputcurrent@VOL (max)				
	DS[2:0]=000	4.9	7.8	11.1	mA
	DS[2:0]=001	7.4	11.7	16.4	mA
	DS[2:0]=010	9.8	15.5	21.7	mA
	DS[2:0]=011	12.2	19.2	26.7	mA
	DS[2:0]=100	14.6	23.0	31.9	mA
	DS[2:0]=101	17.0	26.6	36.8	mA
	DS[2:0]=110	19.4	30.2	41.6	mA
	DS[2:0] =111	21.7	33.7	46.2	mA
John	Highleveloutputcurrent@ VOH (max)				
	DS[2:0]=000	3.6	6.2	9.5	mA
	DS[2:0]=001	5.4	9.3	14.3	mA
	DS[2:0]=010	7.2	12.4	19.1	mA
	DS[2:0]=011	9.0	15.4	23.8	mA
	DS[2:0]=100	10.8	18.5	28.5	mA
	DS[2:0]=101	12.6	21.6	33.1	mA
	DS[2:0]=110	14.4	24.6	37.8	mA
	DS[2:0]=111	16.2	27.7	42.5	mA

2.5.8 18OD33 IO (VDDIO=3.0V) electrical parameters

Applicable domain(VDDIO_EMMC,VDDIO_SD0)

sheet 2 · 10 18OD33IO(VDDIO=3.0V) Electrical parameters

Parameter		Min	Type	Max	Unit
WILL	InputLowvoltage	-0.3		0.25*VDDIO	IN
HIV	InputHighvoltage	0.625*VDDIO		3.3	IN
VT (no pull)	ThresholdvoltagewhenST=0(noschmittrigger)	0.82	0.95	1.11	
VT_PU		0.81	0.93	1.09	IN
VT_PD		0.83	0.96	1.13	
VT+ (no pull)	ThresholdvoltagewhenST=1	1.00	1.10	1.23	IN

Parameter		Min	Type	Max	Unit
VT- (nopull)		0.75	0.90	1.08	
VT+_PU		1.00	1.09	1.21	
VT-_PU		0.73	0.88	1.05	
VT+_PD		1.01	1.11	1.25	
VT-_PD		0.75	0.91	1.09	
~	Input leakage(VI =3.0Vor0V)			+/-10u	A
IOZ	Tri-stateoutputleakagecurrent(VO=3.0Vor0V)			+/-10u	A
RPU	Pullupresistor	33k	60k	93k	Oh
RPD	Pulldownresistor	34k	62k	285k	Oh
VOL	Outputlowvoltage			0.125*VDDIO	IN
VOH	Outputhighvoltage	0.75*VDDIO			IN
IOL	Lowleveloutputcurrent@VOL (max)				
	DS[2:0]=000	3.1	5.5	8.6	mA
	DS[2:0]=001	4.7	8.2	12.7	mA
	DS[2:0]=010	6.2	10.8	16.9	mA
	DS[2:0]=011	7.7	13.4	20.8	mA
	DS[2:0]=100	9.3	16.1	24.9	mA
	DS[2:0]=101	10.8	18.7	28.8	mA
	DS[2:0]=110	12.3	21.2	32.6	mA
	DS[2:0]=111	13.8	23.7	36.3	mA
John	Highleveloutputcurrent@ VOH (max)				
	DS[2:0]=000	5.0	7.5	10.5	mA
	DS[2:0]=001	7.5	11.2	15.7	mA
	DS[2:0]=010	10.1	14.9	21.0	mA
	DS[2:0]=011	12.6	18.6	26.2	mA
	DS[2:0]=100	15.1	22.3	31.4	mA
	DS[2:0]=101	17.6	26.0	36.5	mA
	DS[2:0]=110	20.1	29.8	41.8	mA
	DS[2:0]=111	22.6	33.4	46.9	mA

2.5.9 Audio GPIO electrical parameters

sheet 2 ' 11 AudioGPIO Electrical parameters

Parameter		Min	Type	Max	Unit
WILL	InputLowvoltage	-0.3		0.55	IN
HIV	InputHighvoltage	1.2		1.98	IN
VT+ VT-	Thresholdvoltagewithschmitttrigger	0.8 0.65	0.95 0.82	1.1 0.99	IN
™	Input leakage(VI =1.8Vor0V)			+/-4u	A
IOZ	Tri-stateoutputleakagecurrent(VO=1.8Vor0V)			+/-4u	A
VOL	Outputlowvoltage			0.4	IN
VOH	Outputhighvoltage	1.4			IN
IOL	Lowleveloutputcurrent@VOL (max)	4.9	9.9	18.4	mA
John	Highleveloutputcurrent@ VOH (max)	11.3	17.1	26.1	mA

2.5.10 ETH GPIO electrical parameters

sheet 2 ' 12 ETH GPIO Electrical parameters

Parameter		Min	Type	Max	Unit
WILL	InputLowvoltage	-0.3		0.3*VDD18A	IN
HIV	InputHighvoltage	0.7*VDD18A		1.98	IN
VT+ VT-	Thresholdvoltagewithschmitttrigger	0.84 0.66	0.99 0.83	1.14 1.01	IN
™	Input leakage(VI =1.8Vor0V)			+/-1.3u	A
IOZ	Tri-stateoutputleakagecurrent(VO=1.8Vor0V)			+/-1.3u	A
VOL	Outputlowvoltage			0.4	IN
VOH	Outputhighvoltage	VDD18A-0.4			IN
IOL	Lowleveloutputcurrent@VOL (max) DS=0 Lowleveloutputcurrent@VOL (max) DS=1	8.8 10.2	15.7 17.8	27.3 30.5	mA
John	Highleveloutputcurrent@ VOH (max) DS=0 Highleveloutputcurrent@ VOH (max) DS=1	4.0 4.7	5.3 6.2	7.4 8.5	mA

2.5.11 MIPI Rx electrical parameters

The electrical parameters of MIPID-PHYHighSpeed (MIHS) are shown in Table 2-13 and Table 2-14.

The electrical parameters of MIPID-PHYLowPower (MILP) are shown in Table 2-15 and Table 2-16.

sheet ***13.MIPID-PHYHighSpeed(MISH)2*** difference ***DC*** Electrical parameters

參數	符號	資料速度	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(MIHS)	≤1.5Gbps	70	200	330	mV
		>1.5Gbps				
Internal Termination Resister Value	ZID(MIHS)	≤1.5Gbps	80	100	125	ohm
		>1.5Gbps				
Single-ended threshold for HS termination enable	VTERM-EN(MIHS)	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				

sheet ***2*** ***14.MIPID-PHYHighSpeed (MIHS) differential AC*** electrical parameters

參數	符號	資料速度	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP—VM)	VIDTH(MIHS)	≤1.5Gbps	-70	--	70	mV
		>1.5Gbps	-40	--	40	
Single-ended Input Voltage VP,VM	VIS(MIHS)	≤1.5Gbps	-40	--	460	mV
		>1.5Gbps				
Common-mode interface beyond 450MHz	ΔVCMRX	≤1.5Gbps	--	--	100	mV
		>1.5Gbps				
Common-mode interface 50MHz-450MHz	ΔVCMRX(LF)	≤1.5Gbps	-50	--	50	mV
		>1.5Gbps	-25	--	25	
Single-ended threshold for HS termination enable	VTERM-EN	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				
Common-mode termination	CCM	≤1.5Gbps	--	--	60	pF
		>1.5Gbps				

sheet ***2*** ***15 MIPID-PHYLowPower(MILP)*** difference ***DC*** Electrical parameters

參數	符號	最小值	典型值	最大值	單位
Logic 1 input voltage	VIHLP	740	--	--	mV
Logic 0 input voltage	VILLP	--	--	550	mV
Input hysteresis	VHYST	25	--	--	mV

sheet 2 ' 16 MIPID-PHYLowPower(MILP) Differential AC Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Input pulse rejection	eSPIKE	--	--	300	V·ps
Minimum pulse width response	TMIN-RX	20	--	--	ns
Peak interference amplitude	VINT	--	--	200	mV
Interference frequency	fINT	450	--	--	MHz

2.5.12 Sub-LVDS electrical parameters

The electrical parameters are shown in Table 2-17 and Table 2-18.

sheet 2 ' 17 Sub-LVDS(SL) difference DC Electrical parameters

參數	符號	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(SL)	600	900	1200	mV
Internal Termination Resister Value	ZID(SL)	80	100	120	mV

sheet 2 ' 18 Sub-LVDS(SL) difference AC Electrical parameters

參數	符號	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP—VM)	VIDTH(SL)	-70	--	70	mV
Single-ended Input Voltage VP,VM	VIS(SL)	400	--	1400	mV

2.5.13 HiSPi electrical parameters

HiSPi is divided into SLVS (HSSL) and HiVCM (HSHI), and their respective electrical parameters are shown in Table 2-19 and Table 2-20.

sheet 2 ' 19 HiSPi difference DC Electrical parameters

參數	符號	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(HSSL)	50	200	350	mV
	VCM(HSHI)	660	900	1170	
Internal Termination Resister Value	ZID(HSSL)	80	100	125	mV
	ZID(HSHI)	80	100	125	

sheet 2 ' 20 HiSPi difference AC Electrical parameters

參數	符號	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP—VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	
Single-ended Input Voltage VP,VM	VIS(HSSL)	-40	--	490	mV
	VIS(HSHI)	550	--	1350	

2.5.14 MIPI /LVDS Tx electrical parameters

sheet 2 ' 21 MIPIHSTransmitterDCSpecifications

Symbol	Description	Min	Type	Max	Units	Notes
VCMTX	HStransmitstaticcommon-modevoltage	150	200	250	mV	
|ÿVCMTX(1,0)|	VCMTXmismatchwhenoutputisDifferential-1orDifferential-0	-	-	5	mV	
|VOD|	HS transmit differential voltage	140	200	270	mV	
|ÿVOD|	VODmismatchwhenoutputisDifferential-1orDifferential-0	-	-	14	mV	
VOHHS	HSoutputhighvoltage	-	-	360	mV	
ZOS	Singleendedoutputimpedance	40	50	62.5	Oh	
ÿZOS	Singleendedoutputimpedancemismatch	-	-	20	%	

sheet 2 ' 22 MIPIHSTransmitterACSpecifications

Parameter	Description	Min	Type	Max Units		Notes
ÿVCMTX(HF)	Common-levelvariationsabove 450MHz	-	-	15	mVRMS	
ÿVCMTX(LF)	Common-levelvariationbetween50-450MHz	-	-	25	mVPEAK	
tR andtF	20%-80%risetimeandfalltime	-	-	0.3	UI	1,2
		-	-	0.35	UI	1,3
		100	-	-	ps	4

Note:

1.UIisunitinterval.Example:1UI=1nsfor1Gbpsspeed.
2.ApplicablewhensupportingmaximumHSbitratesÿ 1Gbps(UIÿ 1ns).
3.ApplicablewhensupportingmaximumHSbitrates>1Gbps(UIÿ 1ns)butÿ 1.5Gbps(UIÿ 0.667ns).
4.ApplicablewhensupportingmaximumHSbitratesÿ 1.5Gbps.However,toavoidexcessiveradiation,bitrates<1Gbps(UIÿ 1ns),shouldnotusevaluesbelow150ps.

sheet 2 ' 23 MIPILPTransmitterDCSpecifications

Parameter	Description	Min	Type	Max	Units	Notes
VOH	Theveninoutputhighlevel	1.1	1.2	1.3	IN	1
		0.95	-	1.3	IN	2

Parameter	Description	Min	Type	Max	Units	Notes
VOL	Theveninoutputlowlevel	-50	-	50	mV	-
ZOLP	OutputimpedanceofLPtransmitter	110	-	-	Oh	

Note:

1.ApplicableinnormalLowPowermodewhenthesupporteddatarateÿ1.5Gbps.
2.ApplicableinnormalLowPowermodewhenthesupporteddatarate>1.5Gbps.

sheet 2 ' ***24 MIPILPTransmitterACSpecifications***

Parameter	Description	Min	Type	Max	Units	Notes
TRLP/TFLP	15%-85%risetimeandfalltime	-	-	25	ns	
TREOT	30%-85%risetimeandfalltime	-	-	35	ns	
TLP-PULSE-TX	Minimupulsewidth	20	-	-	ns	
ÿV/ýtSR	Slewrate@CLOAD=0to70pF(FallingEdgeOnly)	30	-	300	mV/ns 1	
		25	-	300	mV/ns 2	
CLOAD	Loadcapacitance	0	-	70	pF	

Note:

1.ApplicableinnormalLowPowermodewhenthesupporteddatarateÿ1.5Gbps.
2.ApplicableinnormalLowPowermodewhenthesupporteddatarate>1.5Gbps.

sheet 2 ' ***25 LVDSTransmitterDC/ ACSpecifications***

Symbol	Description	Min	Type	Max	Units	Notes
YOUR	LVDScommonmodeoffsetvoltage	1.125	1.25	1.375 V		
ÿVOS(1,0)ÿ	VOSmismatchwhenoutputisDifferential-1orDifferential-0	-			mV	
VOD	LVDS transmit differential voltage	247	350	454	mV	
ÿVODÿ	VODmismatchwhenoutputisDifferential-1orDifferential-0	-	-	50	mV	
TRLP/TFLP	15%-85%risetimeandfalltime(DUTside)		-	0.3UI	ns	

2.5.15 SDIO electrical parameters

EMMC/SD0/ SD1 Please refer to 2.5.7 and 2.5.8

2.5.16 VI RAW/BT.601/BT.656/BT.1120 electrical parameters

Please refer to 2.5.7 and 2.5.8 depending on the domain where the IO is located.

2.5.17 **BT.601/BT.656/8080** electrical parameters in **VO (Video out)**

Please refer to 2.5.7 and 2.5.8 depending on the domain where the IO is located.

2.5.18 AUDIO CODEC electrical parameters

sheet ***2 26 AudioCODEC*** Overall indicator table

Parametric	Minimum value	Typical value	Maximum value	Unit	description
Analog Circuit Power Supply **DEPARTMENT**	1.62	1.8	1.98	IN	
VREF		1.4/1.8 *VDD		IN	

sheet ***2 27 AudioDAC*** Electrical parameters

	Minimum value	Typical value	Maximum value	Unit	description
full output amplitude		1.55		Vpp	maximum output signal swing

sheet ***2 28 Audio ADC*** Electrical parameters

	Minimum value	Typical value	Maximum value	Unit	description
maximum input range		1.75		Vpp	maximum input signal swing

2.6 Interface timing

2.6.1 SPI NOR interface timing

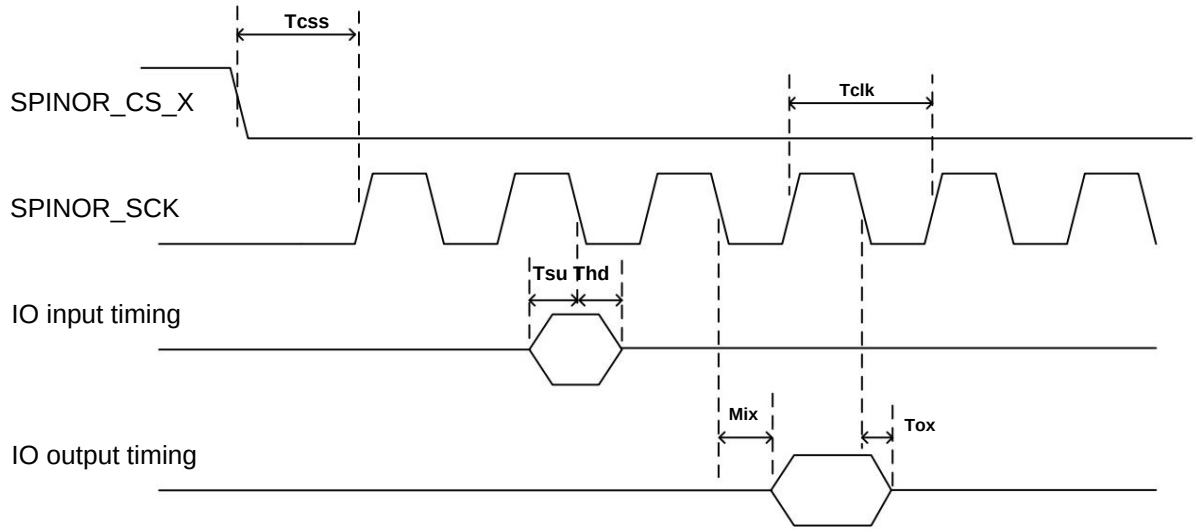


chart *2-7 SPINOR* Interface timing diagram

*IOinputtiming/IOoutputtimng means IOtiming used to transmit SPI_NOR CMD/DATA under 1xI/O, 2xI/O, 4xI/O, which includes SPINOR_SDI, SPINOR_SDOўSPINOR_HOLD_XўSPINOR_WP_X

sheet *2 29 SPI_NOR* Interface timing parameter table

symbol	describe	Minimum general maximum CS			unit
Tcss	Negative edge to first clock edge time 13.4 Clock				ns
Tclk	cycle 13.4 Input signal setup time requirement 3.5				ns
Tsu	Input signal hold time requirement 0 Output signal				ns
Thd	valid delay Output signal hold time				ns
Mix				2.6	ns
TOX		-1.5			ns

2.6.2 SPI NAND interface timing

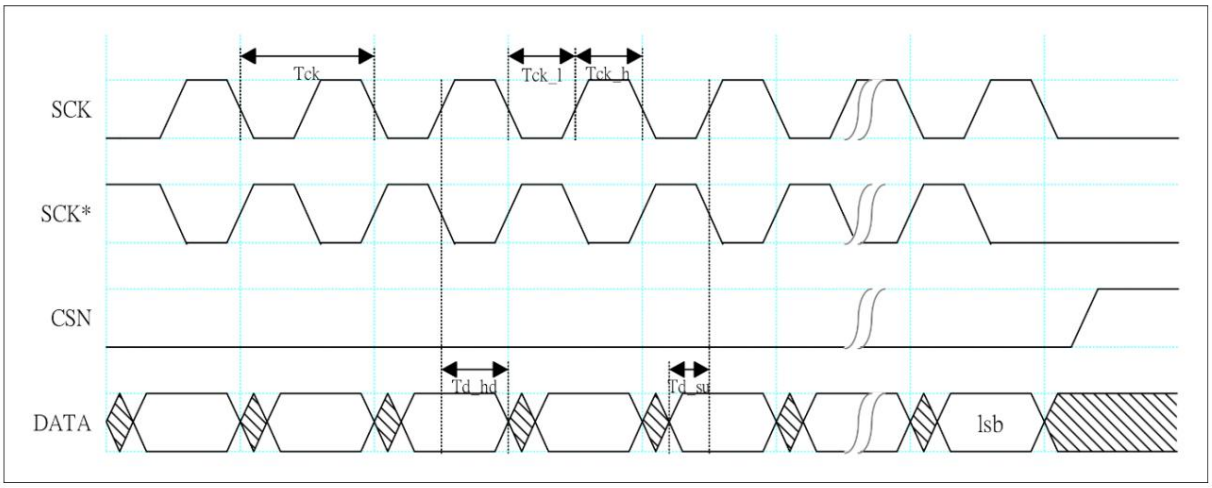


chart **2-8 SPINAND** Input direction timing diagram

sheet **2 30 SPINAND** Input direction timing

	Symbol	Minimum value	Typical value	Maximum value	Unit
Parameter	Tck	10.66		170.56	ns
clock cycle input signal setup time	Td_su	2.00	Td_hd		ns
requirements input signal hold time requirements	1.20				ns

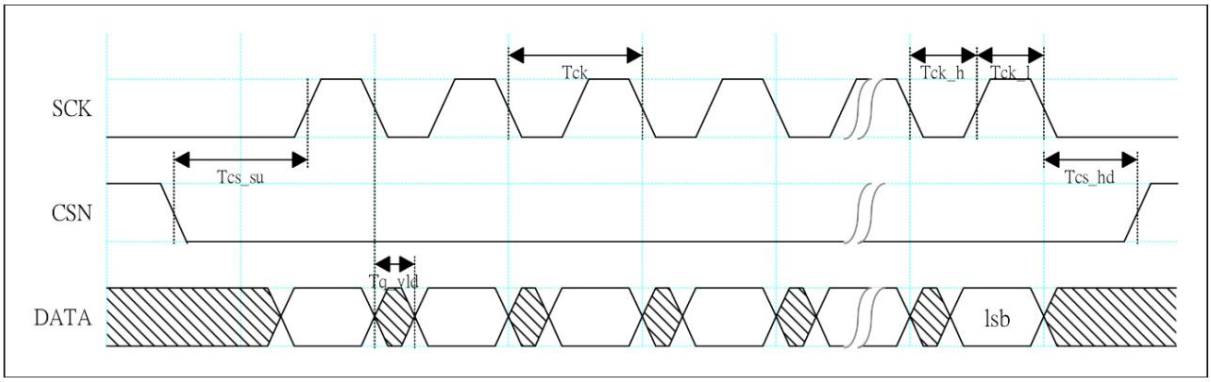


chart **2-9 SPINAND** Output direction timing diagram

sheet **2 31SPINAND** Output direction timing

	Symbol	Minimum value	Typical value	Maximum value	Unit
cycle	Tck	10.66		170.56	ns

	Symbol	Minimum value	Typical value	Maximum value	Unit
high	Tck_h	5.33		85.28	ns
level period clock low	Tck_l	5.33		85.28	ns
level period output **CS**	Tcs_su	10.66	Tcs_hd		ns
setup time output **CS**	10.66	Tq_vld	-1.00		ns
hold time output signal delay				2.00	ns

2.6.3 VI interface timing

The VI interface timing sequence is shown in Figure 2-10.

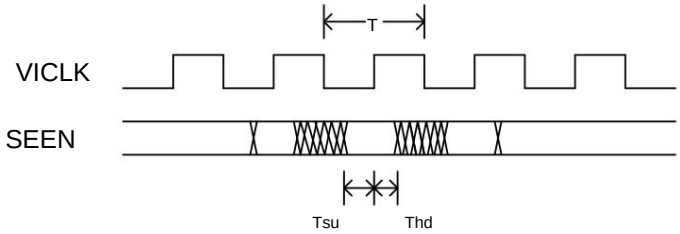


chart *2-10 VI* Interface timing diagram

The VI interface timing parameters are shown in Table 2-32.

sheet *2 32 VI* Interface timing parameter table

	Symbol Min		Type	Max	Unit
VICLKclockcycle	T	6.73			ns
VIDATAsetuptime	Tsu	1.9			ns
VIDATAholdtime Thd		0.8			ns

2.6.4 VO interface timing

The VO interface timing sequence is shown in Figure 2-11.

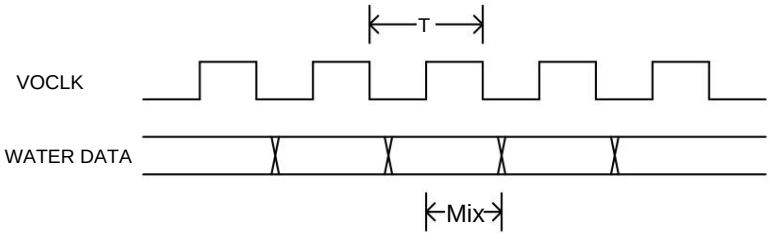


chart *2-11 VO* Interface timing diagram

The VO interface timing parameters are shown in Table 2-33.

sheet **2 33 VO** Interface timing parameter table

	Symbol	Min	Type	Max	Unit
VOCLKclockcycle T			6.73		ns
VODATAdelaytime	Mix	T/2-1.5		T/2+1.5	ns

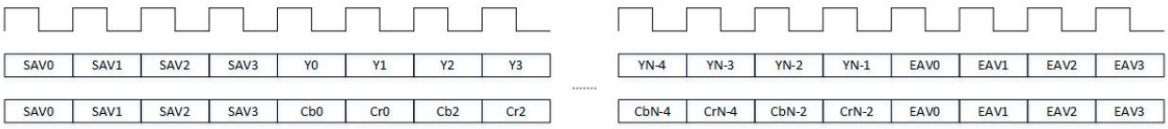


chart **2-12 BT.656** Interface timing diagram

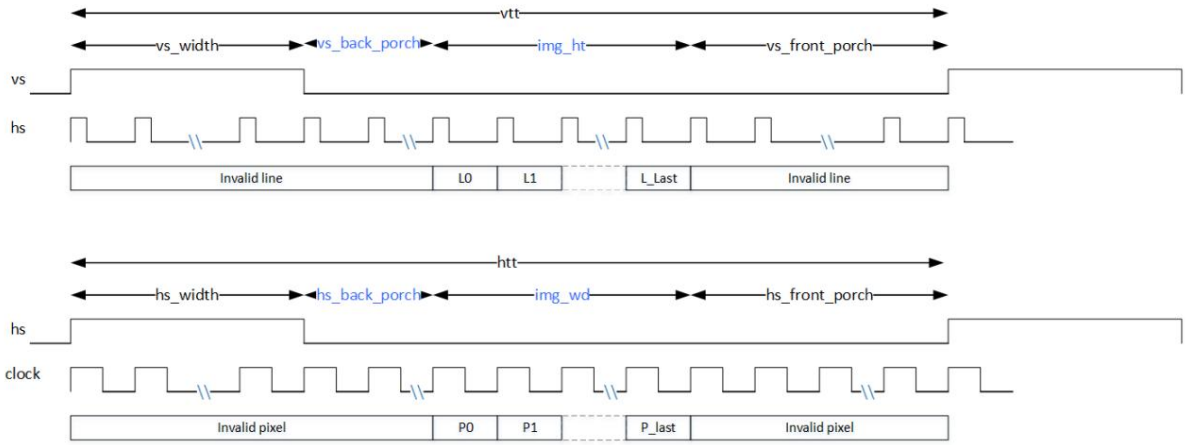


chart **2-13 BT.601** Interface timing diagram

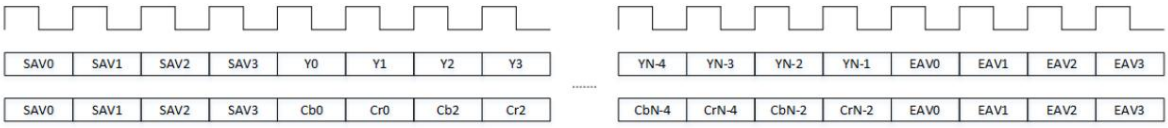


chart **2-14 BT.1120** Interface timing diagram

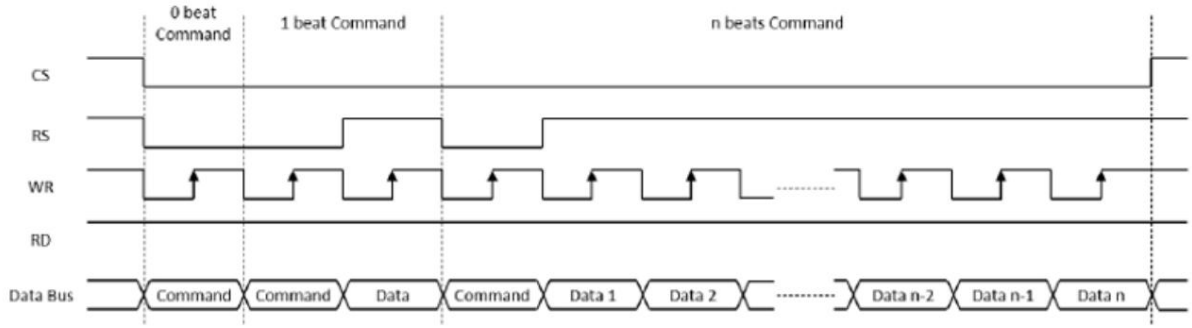


chart *2-15 8080* Interface timing diagram

2.6.5 AIAO (I2S/PCM) interface timing

When external AudioCodec is connected, the interface reception timing in I2S mode and PCM mode is shown in Figure 2-16.

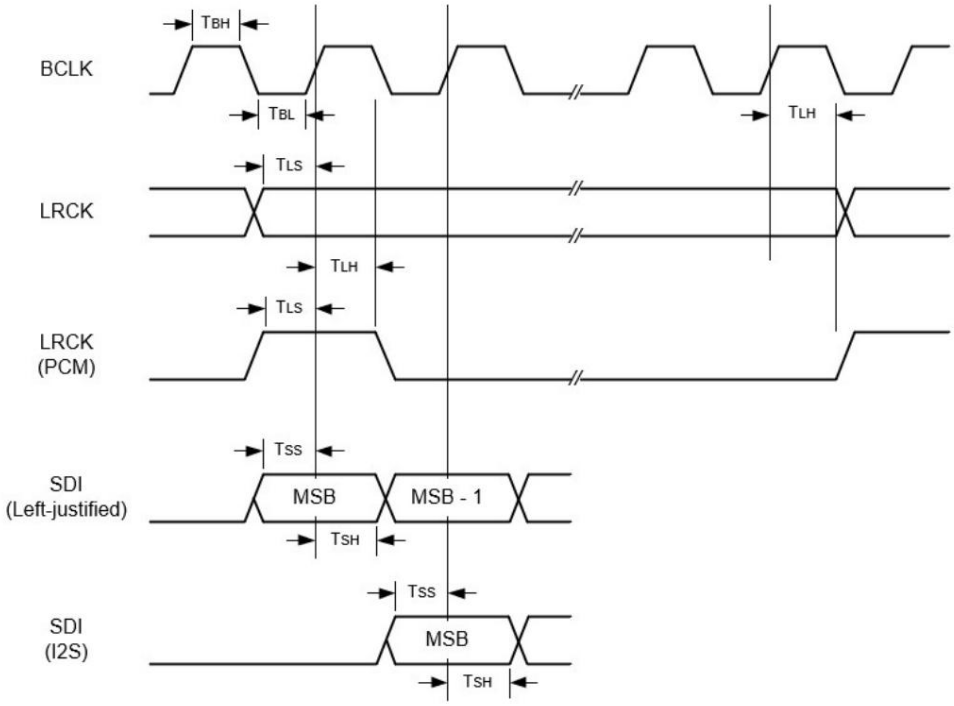


chart *2-16 I2S&PCM* Interface receiving timing diagram

The interface sending timing in I2S mode and PCM mode is shown in Figure 2-17.

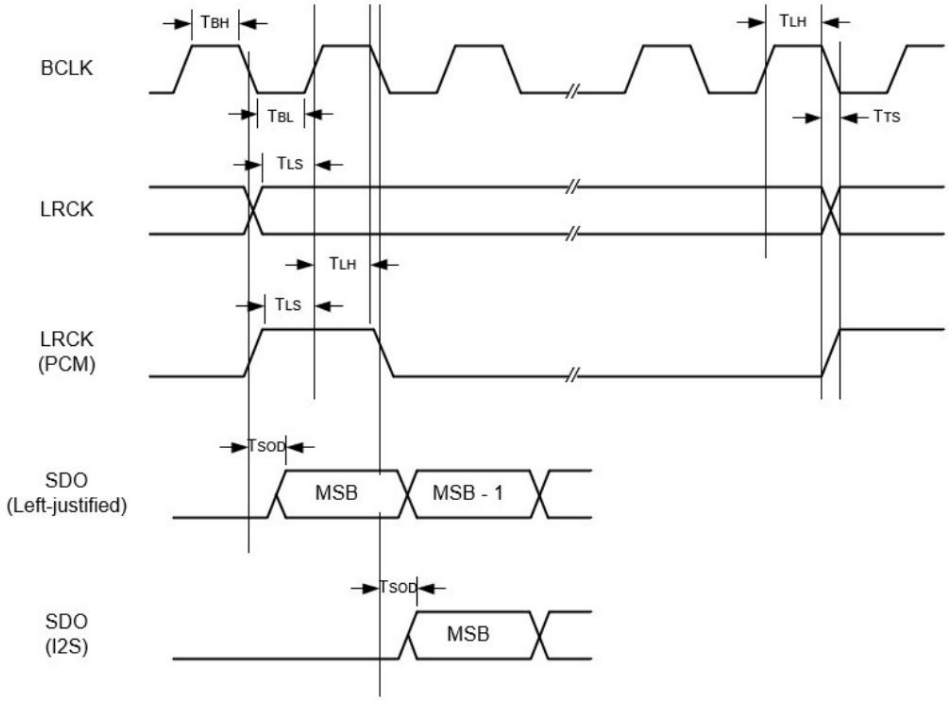


chart ***2-17 I2S&PCM*** Interface sending timing diagram

The interface timing parameters are shown in Table 2-34.

sheet ***34I2S/ PCM 2*** Interface timing parameter table

symbolic parameters		Minimum value	Typical value	Maximum value	Unit
TBL	BCLK low level pulse width (master mode and slave mode)	40	·	·	ns
TBH	BCLK high level pulse width (master mode and slave mode)	40	·	·	ns
TLS	LRCK setup time relative to BCLK rising edge (slave mode)	10	·	·	ns
TLH	LRCK hold time relative to BCLK rising edge (slave mode)	10	·	·	ns
TSS	SDI setup time relative to BCLK rising edge (master mode and slave mode)	10	·	·	ns
TSH	SDI hold time relative to BCLK rising edge (master mode and slave mode)	10	·	·	ns
TTS	BCLK falling edge clock skew relative to LRCK (Master mode)	0	·	10	ns
TSO	SDO signal delay time relative to BCLK falling edge (master mode and slave mode)	0	·	10	ns

2.6.6 I2C interface timing.

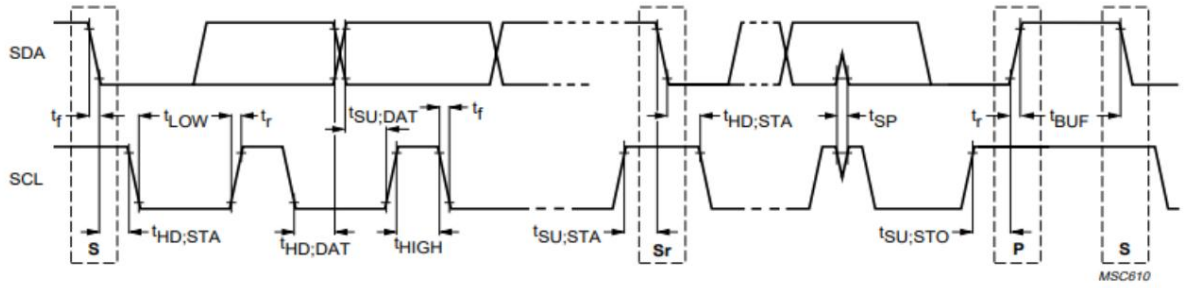


chart **2-18 I2C** Interface timing diagram

sheet **2 35 I2C** Interface timing parameter table

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

2.6.7 SPI interface timing

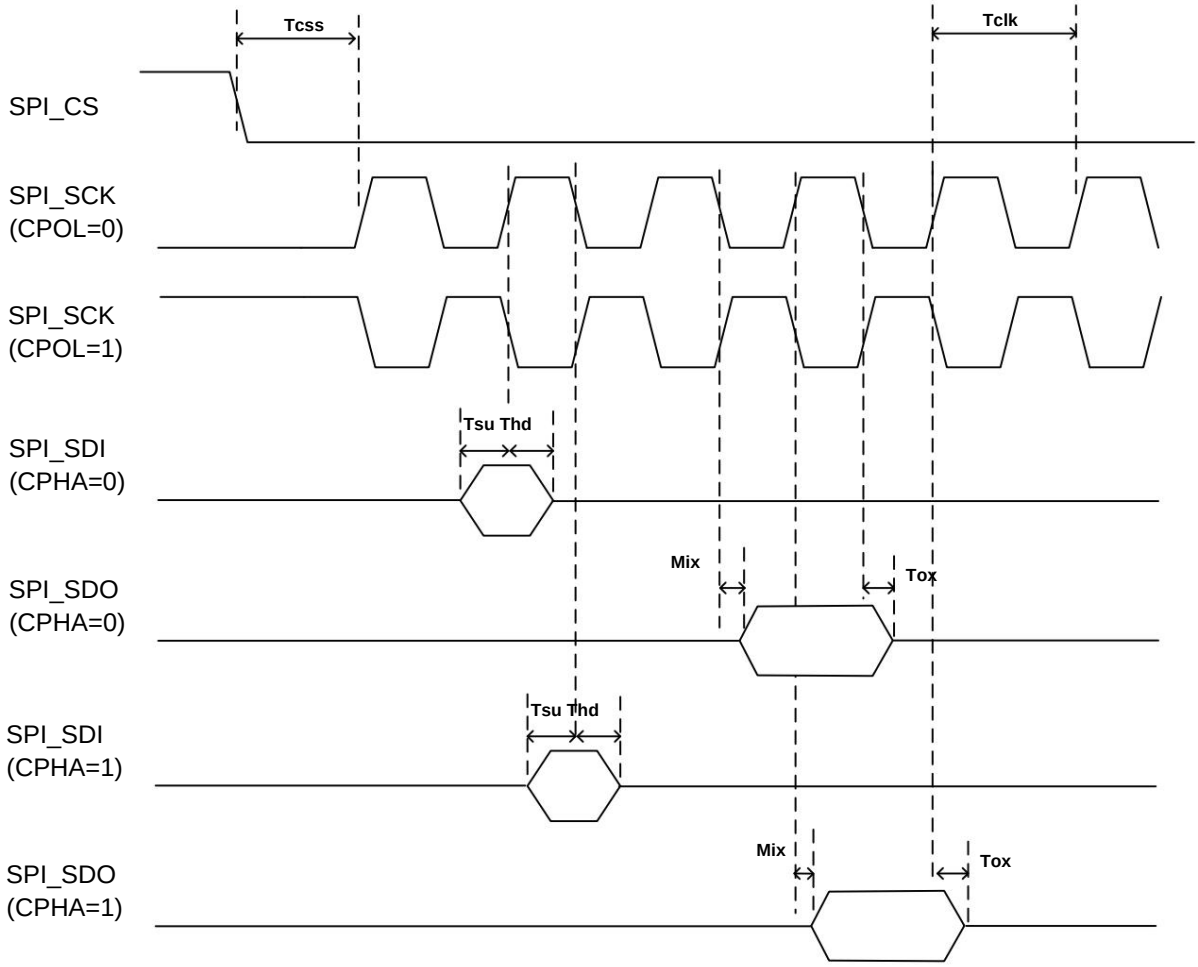


chart *2-19 SPI* Interface timing diagram

sheet *2 36 SPI* Interface timing parameter table

symbol		Minimum value	Typical value	Maximum value	Unit
Fclk	The SCK			46.8	MHz
Tcss	frequency CS is 21.4 from the negative edge to the				ns
Tclk	first clock edge. The clock cycle is 21.4. The input				ns
Tsu	signal setup time requirement is 9.5. The input				ns
Thd	signal hold time requirement is 0. The output				ns
Mix	signal valid delay is the output			3	ns
TOX	signal hold time.	-3			ns

2.6.8 MIPI Rx interface timing

The speed range of MIPIRx is 0.08Gbpsÿdata speedÿ1.5Gbps

A.0.08Gbpsÿdata speedÿ1.5Gbps

The timing diagram is shown in Figure 2-20, and the timing parameters are shown in Table 2-37

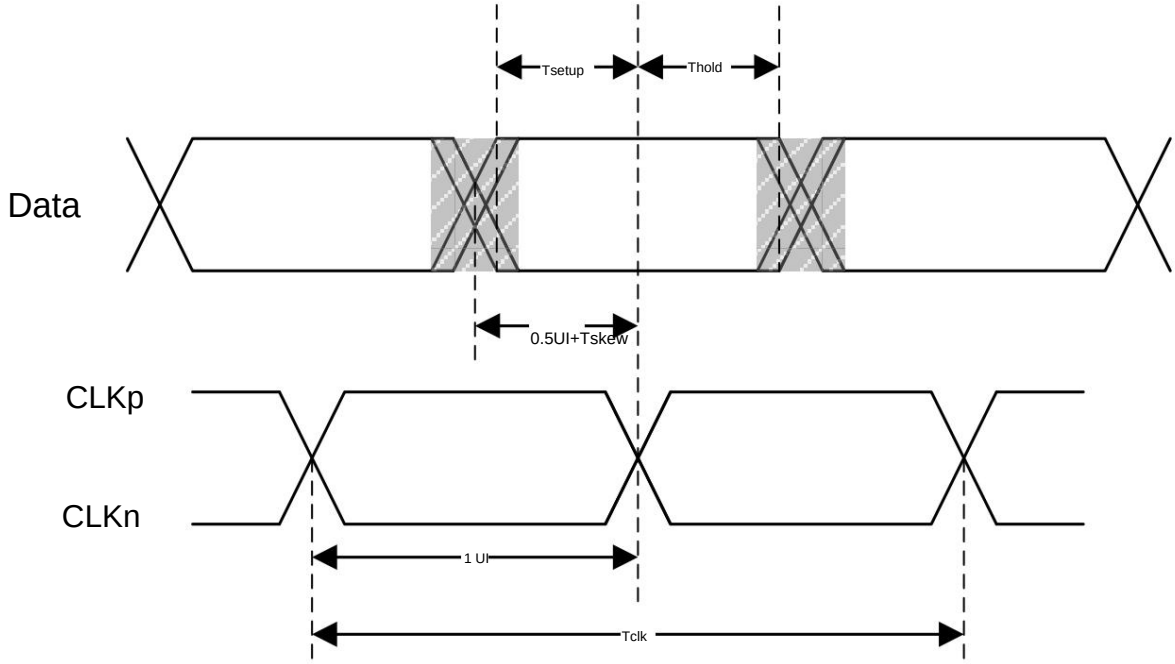


chart ***2-20.MIPIRx*** exist ***0.08Gbps*** ÿdata speedÿ ***1.5Gbps*** clock data timing diagram

sheet ***2 · 37 MIPIRx*** exist ***0.08Gbps*** ÿdata speedÿ ***1.5Gbps*** Timing parameter table

參數	符號	資料速度區間	最小值	典型值	最大值	單位
資料速度	Data Rate	0.08G≤Data Rate≤1G	0.08		1	Gbps
		1G<Data Rate≤1.5G	1		1.5	
差分時鐘週期	Tclk	0.08G≤Data Rate≤1G	2		25	ns
		1G<Data Rate≤1.5G	1.33		2	
發射端資料到時鐘歪斜時間	T_{SKEW}	0.08G≤Data Rate≤1G	-0.15		0.15	UIHS *
		1G<Data Rate≤1.5G	-0.2		0.2	
接收端差分時鐘建立時間	T_{SETUP}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			
接收端差分時鐘保持時間	T_{HOLD}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			
* UIHS= 1/資料速度 = 差分時鐘週期/2						

2.6.9 Sub-LVDS interface timing

The Sub-LVDS clock data timing diagram is shown in Figure 2-21, and the timing parameters are shown in Table 2-38

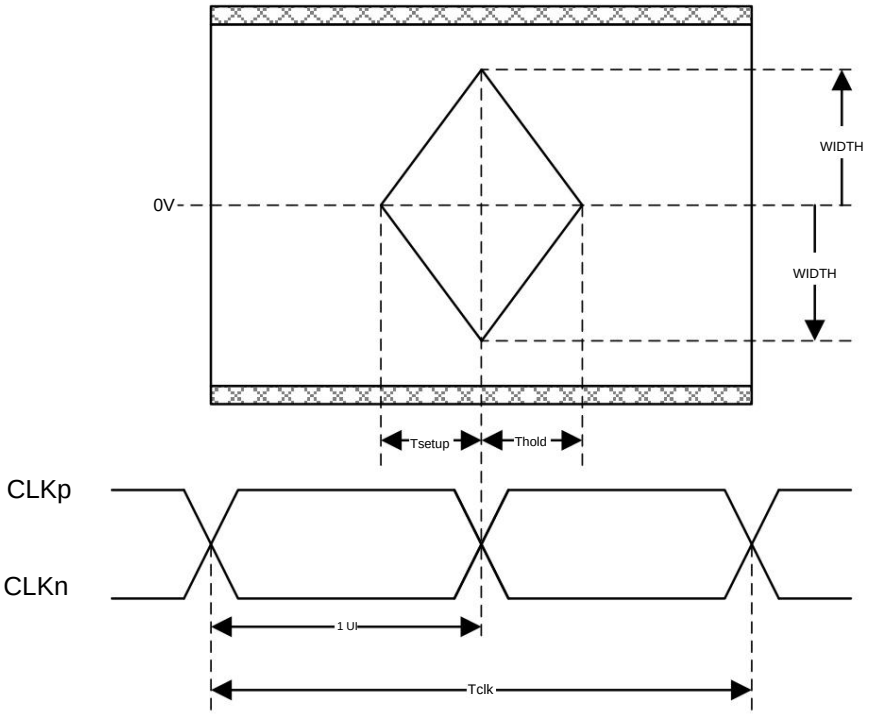


chart *2-21. Sub-LVDS* Clock data timing diagram

sheet *2 38. Sub-LVDS* Timing parameter table

參數	符號	最小值	典型值	最大值	單位
資料速度	Data Rate	--	--	1.5	Gbps
位元標準時間	UI	666.6	--	--	ns
差分時鐘週期	Tclk	1333.3	--	--	ns
接收端差分時鐘建立時間	T_{SETUP}	0.15	--	--	UI
接收端差分時鐘保持時間	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP－VM)	VIDTH(SL)	-70	--	70	mV

* UI= 1/資料速度 = 差分時鐘週期/2

2.6.10 HiSPi interface timing

The HiSPi clock data timing diagram is shown in Figure 2-22, and the timing parameters are shown in Table 2-39

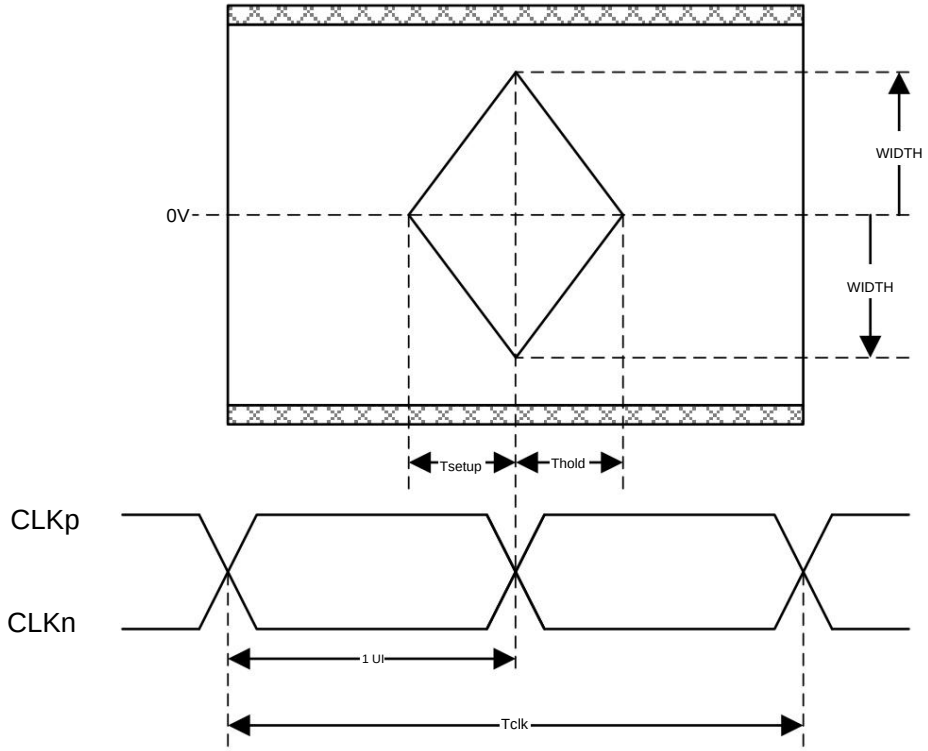


chart *2-22. HiSPi* Clock data timing diagram

sheet *239. HiSPi* Timing parameter table

參數	符號	最小值	典型值	最大值	單位
資料速度	Data Rate	--	--	1.5	Gbps
位元標準時間	UI	666.6	--	--	ns
差分時鐘週期	Tclk	1333.3	--	--	ns
接收端差分時鐘建立時間	T_{SETUP}	0.15	--	--	UI
接收端差分時鐘保持時間	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP－VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	

* UI= 1/資料速度 = 差分時鐘週期/2

2.6.11 MIPI Tx interface timing

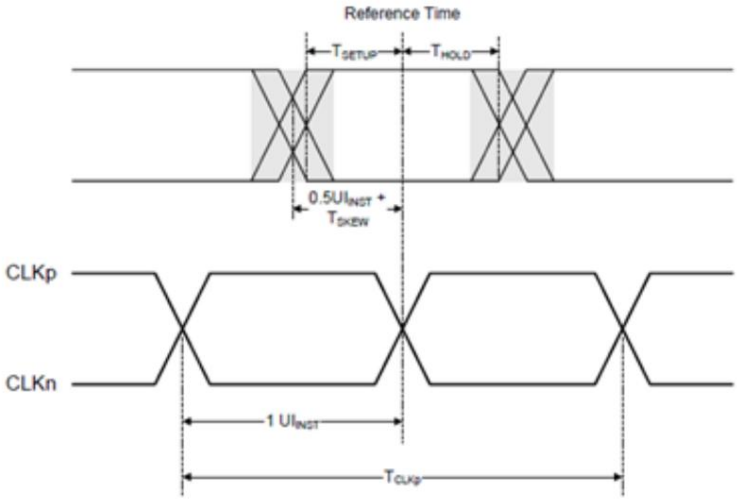


chart *2-23 MIPITX* Interface data versus clock timing diagram

sheet *2 40 Data-ClockTimingSpecificationsfor0.08Gbpsand1Gbps*

Symbol	Description	Min	Name	Max	Units	Notes
TSKEW[TX]	TXDatatoClockSkew	-0.15		0.15	UIHS	

sheet *2 41 Data-ClockTimingSpecificationsfor>1Gbpsand1.5Gbps*

Symbol	Description	Min	Name	Max	Units	Notes
TSKEW[TX]	TXDatatoClockSkew	-0.2		0.2	UIHS	

sheet *2 42 Data-ClockTimingSpecificationsfor>1.5Gbpsand2.5Gbps*

Symbol	Description	Min	Name Max		Units	Notes
TSKEW[TX]	TXDatatoClockSkew	-0.2		0.2	UIHS	
TJX	TXDatatoClockTotalJitter			0.3	UIHS	
DJTX	TXDatatoClockDeterministicJitter			0.2	UIHS	
RJTX	TXDatatoClockRandomJitter			0.1	UIHS	

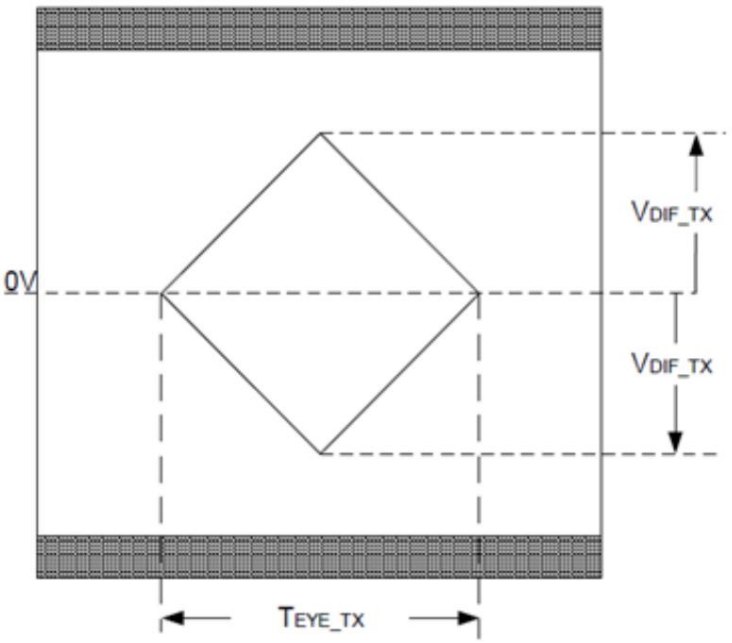


chart ***2-24 TXEYEDiagramSpecification***

sheet ***2 43 TransmitterEyeDiagramSpecification***

Bit Error Rate	TEYE_TX	VDIF_TX
10^{-12}	0.5UI	40mV
10^{-6} (Prorated for Validation)	0.53UI	47mV

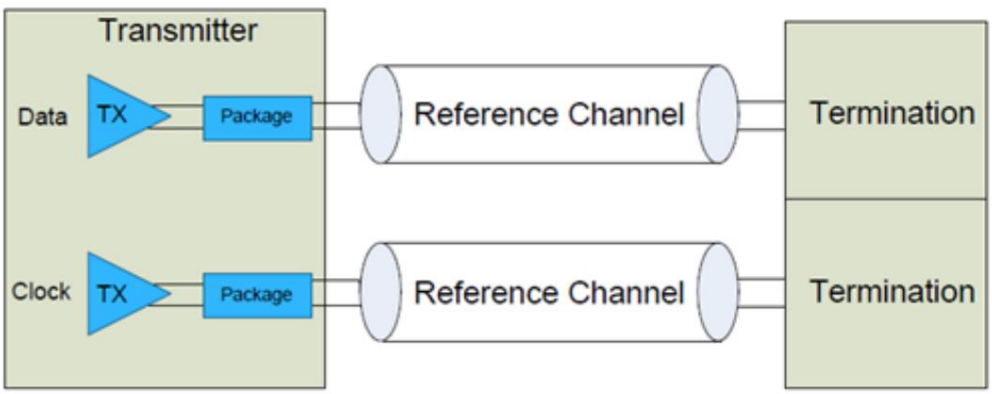


chart ***2-25TransmitterEyeDiagramValidationSetup***

2.6.12 SDIO/MMC interface timing

The data input and output direction timing sequence of a single edge is shown in Figure 2-26.

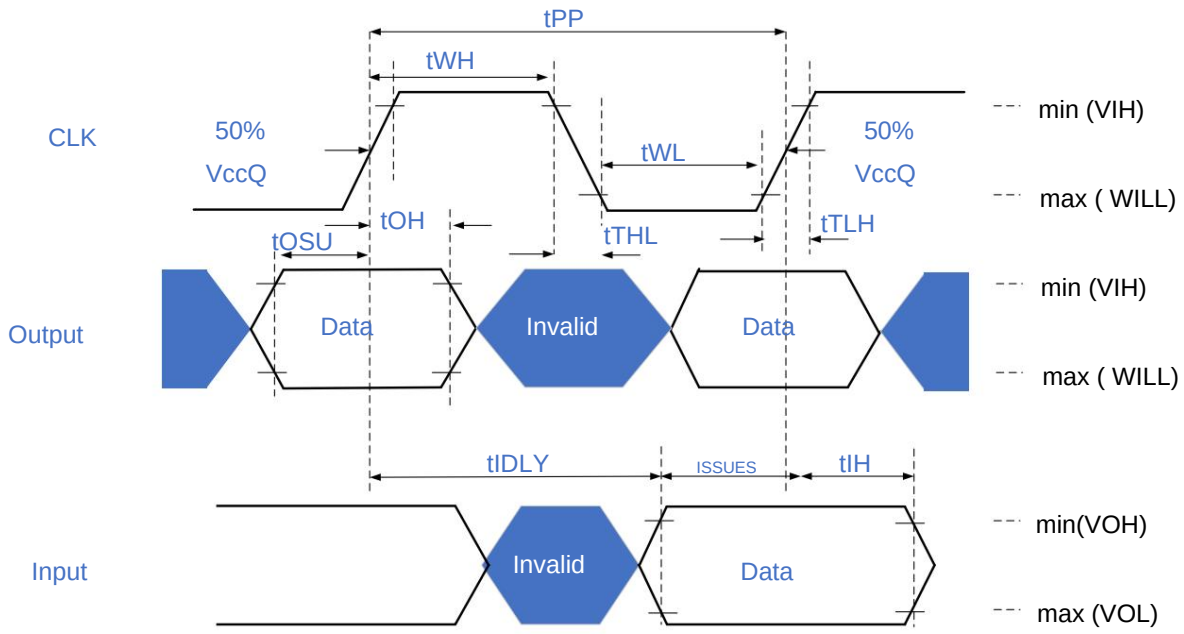


chart *2-26 SDIO/ MMC* single edge *(SDR)* Data input and output timing diagram

sheet *2 44 SDIO/ MMC* single edge *DS(defaultspeed)* Mode timing parameter table

parameter	Symbol	Minimum value	Typical value	Maximum value	Unit	Remarks
ClockCLK						
Clockfrequency Data transfer mode	fPP	0		26	MHz	fpp=1/tpp CLÿ30pF
Clockfrequenyc IdenfificationMode	fOD	0		400	KHz	CLÿ30pF
Clockhightime	tWH	10			ns	CLÿ30pF
Clocklowtime	tWL	10			ns	CLÿ30pF
Clockrisetime	tTLH			10	ns	CLÿ30pF
Clockfalltime	tTHL			10	ns	CLÿ30pF
InputsCMD,DAT(referencedtoCLK)						
Inputset-uptime	ISSUES	6			ns	CLÿ30pF
Inputholdtime	tIH	8.3			ns	CLÿ30pF
OutputsCMD,DAT(referencedtoCLK)						

parameter	Symbol	Minimum value	Typical value	Maximum value	Unit	Remarks
Outputset-uptime tOSU 5					ns	CLÿ30pF
Outputholdtime tOH 5					ns	CLÿ30pF

sheet ***45 SDIO/ MMC2*** single edge ***HS(Highspeed)*** Mode timing parameter table

parameter	Symbol	Minimum value	Typical value	Maximum value	Unit	Remarks
ClockCLK						
Clockfrequency Data transfer mode	fpp	0		52	MHz	fpp=1/tpp CLÿ30pF
Clockhightime	tWH 6.5				ns	CLÿ30pF
Clocklowtime	tWL 6.5				ns	CLÿ30pF
Clockrisetime	tTLH			3	ns	CLÿ30pF
Clockfalltime tTHL				3	ns	CLÿ30pF
InputsCMD,DAT(referencedtoCLK)						
Inputset-uptime tISU		6			ns	CLÿ30pF
Inputholdtime	tIH	2.5			ns	CLÿ30pF
OutputsCMD,DAT(referencedtoCLK)						
Outputset-uptime tOSU 6					ns	CLÿ30pF
Outputholdtime tOH 3					ns	CLÿ30pF

The data input and output direction timing sequence of double edges is shown in Figure 2-27.

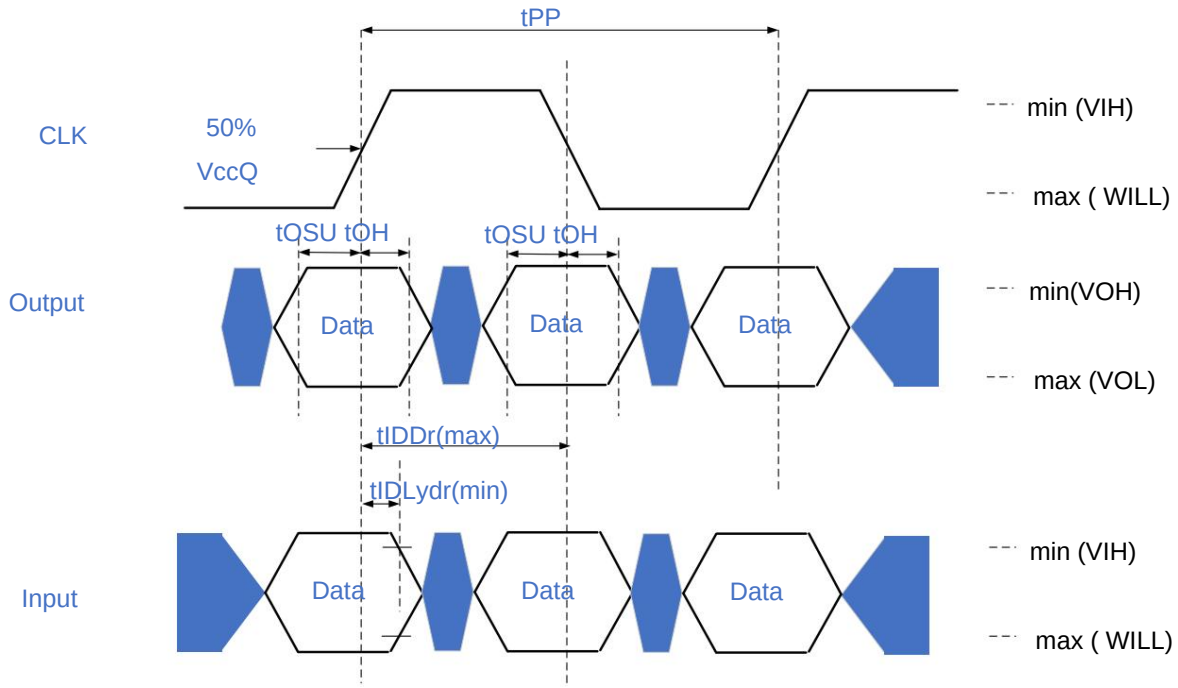


chart ***2-27 SDIO/ MMC*** Double edge ***DDR50*** Pattern data input and output direction timing diagram

sheet *46 SDIO/ MMC2* Double edge *DDR50* Mode timing parameter table

parameter	symbol	most Small value	typical value	most big value	Unit	remarks
ClockCLK						
ClockfrequencyDatatransferMode	fP	0		52 MHz		fpp=1/tpp CLÿ30pF
InputsDAT(referencedtoCLK)						
Input delay time during data transfer	tIDLYDr 1.5			7	ns	CLÿ20pF
OutputsDAT(referencedtoCLK)						
Outputset-uptime	tOSU	3			ns	CLÿ20pF
Outputholdtime	tOH	2.5			ns	CLÿ20pF

The data input and output direction timing sequences of HS200 and SDR104 are shown in Figure 2-28.

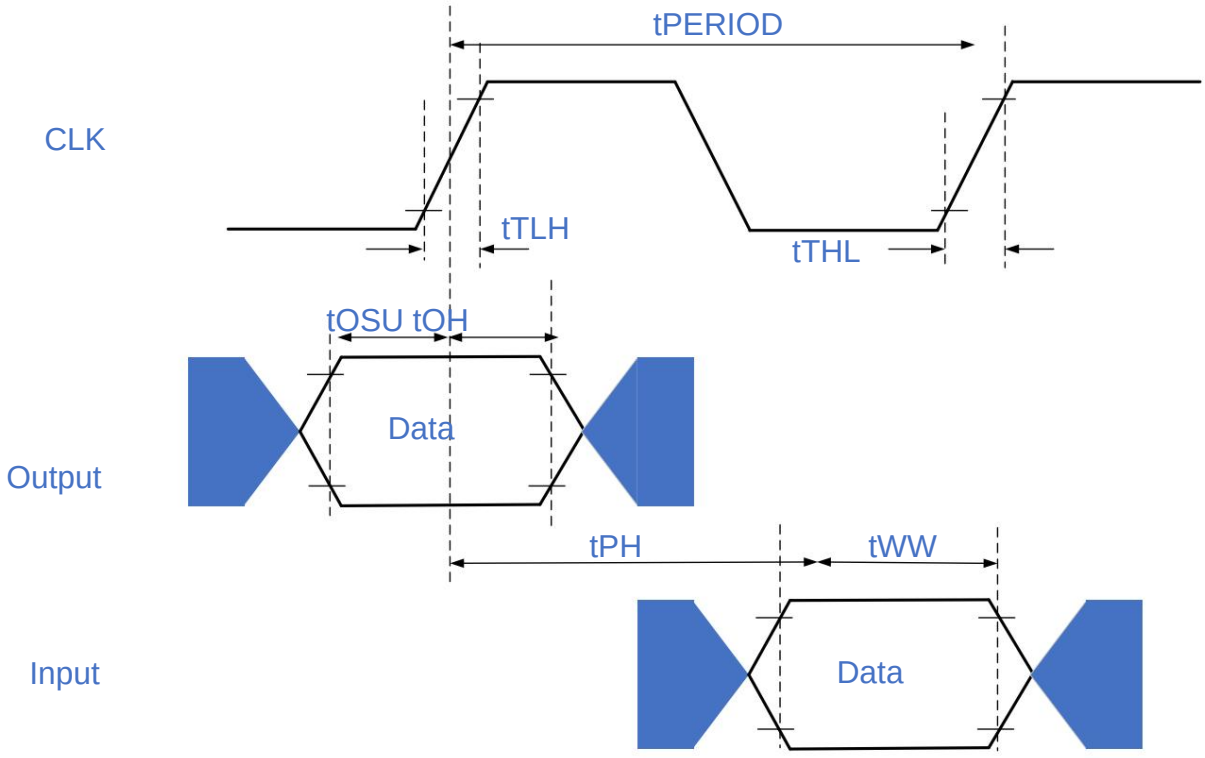


chart *2-28 SDIO/ MMCHS200* and *SDR104* Pattern data command output direction timing diagram

sheet *2 47 SDIO/ MMCHS200* and *SDR104* Mode output parameter table

parameter	symbol	smallest value	Typical value	Maximum value	Unit	Remarks
Outputset-uptime	TOSU 1.4	-			ns	CDEVICEÿ6pF

parameter	symbol	smallest value	Typical value	Maximum value	Unit	Remarks
Outputholdtime	tOH	0.8	-		ns	

sheet **2** ***48 SDIO/ MMCHS200*** and ***SDR104*** Mode input timing parameter table

parameter	symbolic	minimum	typical value	Maximum value	unit	remarks
PhasedifferencebetweendeviceTX CMD/DATandRXCLK	tPH	0		2	UI	UnitInterval(UI)isonebitnominaltime.For200Mhz,UI=5ns
Inputvaliddatawindow	tWW	0.575			UI	TVW=2.88nsat200MHz